AS1454/44/34/24 — 9-72VDC / 24VAC Digital Power SoCs with Integrated GreenEdge™ 2kV Isolation & Quad Outputs

GENERAL DESCRIPTION

The AS14x4 devices are Quad-Output Digital Power SoCs for 9.5-72VDC & 24VAC isolated power applications. All are built on Akros' integrated *GreenEdge*™ 2kV digital isolation technology creating a flexible power platform that eliminates all opto-couplers and minimizes component count and design footprint.

Synchronous converters with digital loop and timing control are integrated with digital isolation as part of an advance power system architecture for high-efficiency and cost-effective designs. Selectable spread-spectrum clocking on all PWMs reduces the power supply spectral noise for superior EMC performance. Bi-directional Isolated GPIO and isolated ADC ease system level design in many industrial applications.

A Software compatible I^2C management interface (AS1434 & AS1454 only) provides advanced power control and diagnostics capability. Hardware (pin) programmable device operation is available on all four devices.

TYPICAL APPLICATIONS

- Surveillance Cameras and Building Management Systems
- Automotive Power and Infotainment Systems
- Industrial Equipment
- Telecom Backplane and Distributed Power Systems
- Multi-rail Isolated Flyback and Forward Power Supplies

ORDERING INFORMATION

The AS14x4 family is comprised of four pin-compatible devices, all available in 64-lead QFN Reduction of Hazardous Substance (RoHS) compliant packages.

Part #	Hardware Mode	Software (I^2C) Mode	Iout_1,4 (each)	Iout_2,3 (max, each)
AS1424	x		Set Externally	1.25 ARMS
AS1434	x	x	Set Externally	1.25 ARMS
AS1444	x		Set Externally	2.0 ARMS
AS1454	x	x	Set Externally	2.0 ARMS

FEATURES

Primary-Side DC-DC Controller

- High-efficiency DC-DC Controller with Digital Optimization
- Integrated Primary-Secondary High-Voltage 2kV Digital Isolation
- Programmable Primary Clock Frequency

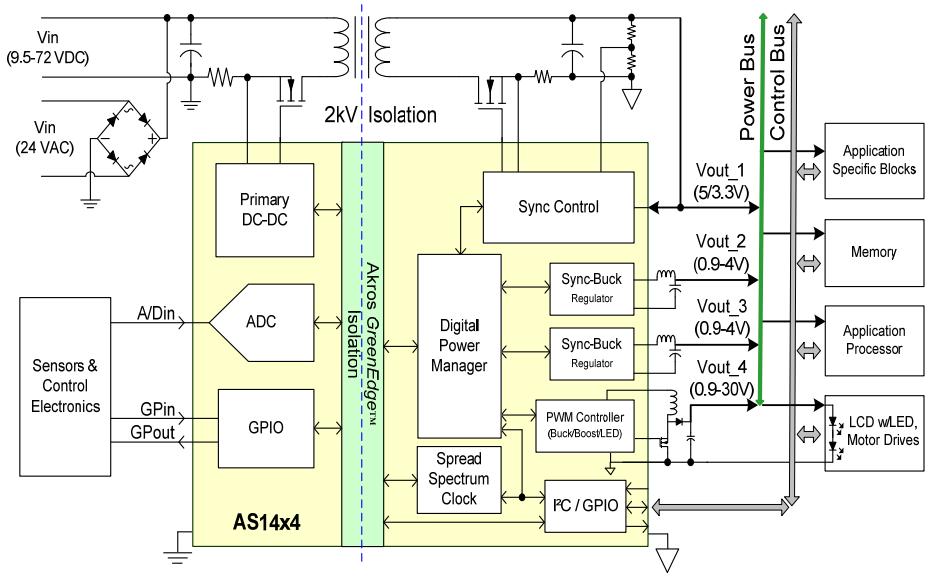
Secondary-Side Power Outputs

- Output #1: Sync Controller with programmable power-FET timing for high efficiency at both light and full loads
- Outputs #2, #3: Fully integrated Buck Regulators with 2A or 1.25A FETs
- Output #4: DC-DC Controller for Buck, Boost, or LED Driver
- High current capability on Outputs #1 and #4

EMC Compliance and Protection

- Synchronous spread-spectrum clocking on all PWMs
- Meets UL60950 and UL1577 requirements for basic

SIMPLIFIED APPLICATION DIAGRAM



Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250, San Jose, CA 95119 USA
408.746.9000 ▪ http://www.AkrosSilicon.com

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PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1 - AS14x4 Pin Assignments

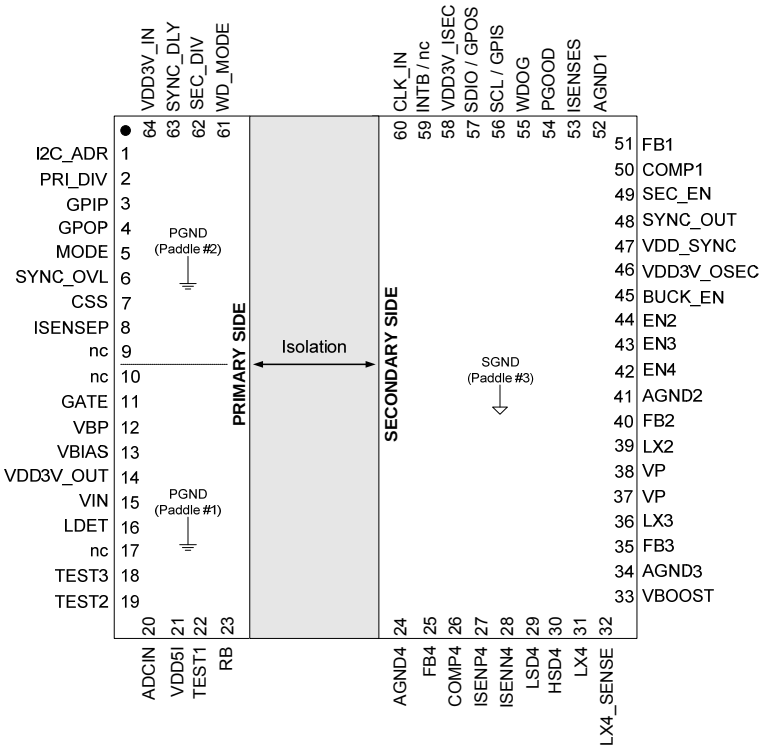


Table 1 - AS14x4 Signal Descriptions - Primary Side

Pin	Name	I/O[1]	Description
Primary-Side: Common Power Pins			
15	VIN	P	AS14x4 startup power input.
Paddle #1, Paddle #2	PGND	P	Input power and Primary Side Transformer grounds. Two of three bottom side device connections (Paddles #1, #2), PGND is the Primary Side ground.
16	LDET	A, I	Voltage detects input. Must be 2.4 VDC (min) below VIN, (see Electrical Characteristics).
12	VBP	P	Internal bias node, decouple with an external capacitor to VBIAS.
13	VBIAS	P	Bias voltage input (typically from a power transformer winding), used after power-up of VIN complete.
14	VDD3V_OUT	P	Primary-side supply voltage source (3.3 volts). This supply can be used for additional external circuits on the primary side that are referenced to PGND, see Electrical Characteristics for supply limits.
64	VDD3V_IN	P	Primary-side input supply voltage (3.3 volts) normally connected to VDD3_OUT.
21	VDD5I	P	Internal 5V generator bias node that can be used to supply PGND referenced devices, see Electrical Characteristics for supply limits. Must be decoupled with an external capacitor to PGND.
23	RB	I, PU	High voltage power control node, decouple with external capacitor to PGND.
Primary-Side: DC-DC Controller			
7	CSS	A	Primary-side PWM Soft Start input, decouple with external capacitor to PGND.
11	GATE	A	Primary-side external power FET gate drive.
8	ISENSEP	A	Current sense input, also used to set Primary PWM current limit (with external resistor).

63	SYNC_DLY	A	Along with SYNC_OVL this signal sets Primary and Secondary side primary sync delay timing for Output #1. Connecting a resistor to primary ground (PGND) from this input will optimize output efficiency for a given power level or power-FET choice. See Table 15 for resistor value selection and other details. In addition, decouple with a cap to PGND.
6	SYNC_OVL	A	Along with SYNC_DLY this signal sets Primary and Secondary-side primary sync overlap timing for Output #1. Connecting a resistor to primary ground (PGND) from this input will optimize output efficiency for a given power level or power-FET choice. See Table 15 for resistor value selection and other details. In addition, decouple with a cap to PGND.
Primary-Side: Clock Dividers			
2	PRI_DIV	A, I	Primary PWM frequency divider input. Connect an external resistor (5%) from this input to primary ground (PGND) to set the Primary PWM clock divider for either internal or external (if the CLK_IN input is active) clocking operation. The Primary PWM clocking rate is a function of both PRI_DIV and SEC_DIV divider ratios. See Device Description, Figure 3 and Table 13 for details.
62	SEC_DIV	A, I	Secondary PWM frequency divider input. Connect an external resistor (5%) from this input to primary ground (PGND) to set the Secondary PWM clock divider for either internal or external (if the CLK_IN input is active) PWM clocking operation. The Secondary PWM clocking rate is a function of this SEC_DIV divider ratio. See Device Description, Figure 3 and Table 13 for details.
Primary-Side: Inputs & Outputs			
3	GPIP	I, PU	General-purpose digital input on primary side, referenced to PGND.
4	GPOP	O	General-purpose digital output on primary side, referenced to PGND.
20	ADCIN	A, I	General purpose ADC input, referenced to PGND.
1	I2C_ADR	A, I	I^2C Interface Device Address select. I2C_ADR sets the AS1454/34 device address. One of 8 possible Device addresses is configured by connecting a resistor on this input to primary ground (PGND). As a result of the chosen resistor, 3 bits of available addressing for the device are configured. See Table 18 for values and other details.
61	WD_MODE	I	Watchdog Timer mode. Enables/disables watchdog timer and sets timer period, operation also varies with MODE input setup. **For Hardware Mode Operation (all AS14x4 devices):** WD_MODE = Low (connect to PGND): watchdog off. WD_MODE = Capacitor to PGND: A 1 second timeout generates a PGOOD output transition. WD_MODE = High (connect to VDD3V_OUT): A 32 second timeout generates a PGOOD output transition. **For Software Mode Operation (AS1454 or AS1434 only):** WD_MODE = Low (connect to PGND): watchdog off. WD_MODE = Capacitor to PGND: Power-on enables watchdog usage and counter starts (at max count) after PGOOD indicates good power. Use the Watchdog Timeout Register to change timeout count. Watchdog servicing is via Hardware or I^2C commands. WD_MODE = High (connect to VDD3V_OUT): Power-on enables watchdog usage but waits for software to enable before starting. Use Watchdog Timeout Register for timeout length (reset to max). Watchdog servicing is via Hardware pin or I^2C commands.

5	MODE	I	The MODE pin selects the device operation mode at power-on. **For Hardware Mode Operation (all AS14x4 devices):** – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to PGND). – Mode 2 = HW Operating Mode o Mode 2 is selected with a pull-up resistor (17.8KΩ max) from MODE to VDD3V_OUT plus a required power-on reset capacitor from MODE to PGND. **For Software Mode Operation (AS1454 or AS1434 only):** – Mode 1 = Reset mode o Mode 1 is selected by holding the MODE pin Low (MODE to PGND). – Mode 2 = SW Operating Mode with I²C device address per I2C_ADR pin setting o Mode 2 is selected with a required power-on reset capacitor from MODE to PGND.
22	TEST1	A	Factory test control. For normal operation connect to Paddle #1 (PGND) through a 100KΩ resistor.
19	TEST2	A	Factory test control. For normal operation connect to Paddle #1 through a 75KΩ resistor.
18	TEST3	A	Factory test control. For normal operation connect to Paddle #1 (PGND).
9, 10, 17	nc		No User Connection. Must be floated.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

Table 2 - AS14x4 Signal Descriptions - Secondary Side

Pin	Name	I/O[1]	Description
Secondary-Side: Common Power and Setup			
Paddle #3	SGND	P	Secondary-side ground connection. One of three bottom side device connections, SGND (Paddle #3) is the secondary-side ground connection.
37, 38	VP	P	#2, #3, #4 DC-DC regulators and controller power inputs, internally connected together. Must be connected externally to the same source, nominally Output #1.
46	VDD3V_OSEC	P	Internal Buck power regulator output. Must be decoupled and used for VDD3V_ISEC (pin 58) power source. VDD3V_OSEC can also be used for additional 3.3V secondary-side platform power (pull-ups, etc.); see Electrical Characteristics for supply limits.
58	VDD3V_ISEC	P	Secondary-side 3.3V power input. This must be sourced from VDD3V_OSEC (pin 46).
49	SEC_EN	I, PU	Secondary-side Enable. A capacitor on this input to SGND is required.
Secondary-Side: Synchronous Rectification Controller (Output #1)			
47	VDD_SYNC	A	Controller Sync FET power decoupling node. Decouple with an external capacitor, VDD_SYNC to SGND. This node is nominally 5V.
51	FB1	A	Controller voltage feedback input.
53	ISENSES	A	Controller secondary-side sync switches node current sense. Sensed signal is used to control the external secondary-side power FET, making it an efficient power diode.
50	COMP1	A	Controller compensation network connection.
48	SYNC_OUT	A	Controller sync gate drive output. Used for secondary-side synchronization in conjunction with the primary-side controller.
52	AGND1	P	Controller secondary-side sense ground, used for both differential feedback and differential current sensing. Should be routed differentially, as the pairs of FB1 & AGND1 and ISENSES & AGND1.
Secondary-Side: Regulator (Output #2)			
41	AGND2	P	Sense ground for the Output #2, should be routed together with FB2 for differential feedback sensing and then tied to ground at the feedback resistor. If Output #2 is not used, AGND2 should still be tied to SGND.
39	LX2	A	Regulator switches node output. If Output #2 is not used, float LX2 (no user connection).
40	FB2	A	Regulator voltage feedback input, also used to disable Output #2 (see EN2).
44	EN2	D, I, PU	Hardware enables control for Regulator #2. A capacitor to ground applied to this input is required for buck reset before start up. This capacitor also sets the regulator delay start time, complimenting the internal fixed soft-start time. If Output #2 is not used, apply a Low (SGND) to this input, and connect FB2 to VP to fully disable the regulator.
Secondary-Side: Regulator (Output #3)			
34	AGND3	P	Sense ground for the Output #3, should be routed together with FB3 for differential feedback sensing and then tied to ground at the feedback resistor. If Output #3 is not used, AGND3 should still be tied to SGND.
36	LX3	A	Regulator switches node output. If Output #3 is not used, float LX3 (no user connection).
35	FB3	A	Regulator voltage feedback input, also used to disable Output #3 (see EN3).
43	EN3	D, I, PU	Hardware enables control for Regulator #3. A capacitor to ground applied to this input is required for buck reset before start up. This capacitor also sets the regulator delay start time, complimenting the internal fixed soft-start time. If Output #3 is not used, apply a Low (SGND) to this input, and connect FB3 to VP to fully disable the regulator.

Secondary-Side: Buck or Boost Controller (Output #4)			
45	BUCK_EN	D, I	Selects between Buck and Boost mode of operation for Output #4. Low = SGND = Boost. High = Buck If Output #4 is not used, tie BUCK_EN to SGND.
33	VBOOST	A	Controller Boost voltage decoupling node. Decouple with a capacitor to LX4 when Output #4 is in Buck mode. When operating Output #4 in Boost mode, this input should be connected to Output #1. If Output #4 is not used, VBOOST should be tied to VP.
30	HSD4	A	Controller High Side external Power FET gate Drive. If Output #4 is not used HSD4 should be left floating with no user connection.
29	LSD4	A	Controller Low Side external Power FET gate Drive. If Output #4 is not used LSD4 should be left floating with no user connection.
24	AGND4	P	Sense ground for Controller #4, together with FB4 used for differential feedback sensing at the feedback divider. If Output #4 is not used, AGND4 should still be tied to SGND.
27	ISENP4	A	Positive current sense input. If Output #4 is not used, ISENP4 should be tied to SGND.
28	ISENN4	A	Negative current sense input. If Output #4 is not used, ISENN4 should be tied to SGND.
25	FB4	A	Controller voltage feedback input, also used to disable Output #4 (see EN4).
42	EN4	D, I, PU	Enable control for Controller #4. A capacitor to ground applied to this input is required for proper Controller #4 power-on reset and start up. This capacitor also sets the controller delay start time, complimenting the internal fixed soft-start time. If Output #4 is not used, apply a Low (SGND) to this input, and connect FB4 to VP to fully disable the controller.
26	COMP4	A	Controller compensation network connection. If Output #4 is not used COMP4 should be left floating with no user connection.
31	LX4	A	Controller switches node output. If not used (typical for Boost and LED Boost applications) LX4 should be tied to SGND.
32	LX4_SENSE	A	Remote sense for LX4, used for differential sensing. Should be routed differentially with LX4 (Buck mode). If not used (typical for Boost and LED Boost applications) LX4_SENSE should be tied to SGND.
Secondary-Side: I^2C Interface (or I/O in Hardware Mode)			
57	SDIO / GPOS	OD	SDIO in Software mode, used for I^2C bi-directional data input/output. GPOS in Hardware mode, this output reflects the GPIP pin state (from the primary side).
56	SCL / GPIS	I / I	SCL in Software mode, used as the I^2C clock input. GPIS in Hardware mode is an input that drives the GPOP pin state (on the primary-side).
59	INTB / nc	OD	NTB in Software Mode. The I^2C interface interrupts output, active low. The open drain output allows user defined voltage output high level. Hardware Mode: No user connection. Leave open.
Secondary Side: External PWM Clock Sync Input			
60	CLK_IN	I, PU	DC coupled clock input for timing of Primary and Secondary DC-DC regulators & controllers if synchronizing to an external time source is desired. Nominally sourced from the local Ethernet master clock.

Secondary Side: Additional Inputs and Outputs			
54	PGOOD	OD	Logical “AND” of global power good & watchdog status. High = All enabled voltages (#1 with any or all of #2, #3, and #4) are within voltage spec and there is presently no watchdog timeout. Low = one or more of enabled voltages out of spec, or, the watchdog has timed out. Note that PGOOD operation is different for Hardware and Software modes of operation (selected by the MODE input). For Hardware mode PGOOD operation details see “
55	WDOG	I	Watchdog timer input for hardware reset of watchdog timer (if enabled). Serviced with a transition of either polarity.

[1] I = Input, O = Output, I/O = Bidirectional, PU = Internal pull-up, PD = Internal pull-down, P = Power, A = Analog, D = Digital, OD = Open drain

TEST SPECIFICATIONS

Table 3 - Absolute Maximum Ratings

Parameter	Max	Unit
VIN: to PGND	100 [1]	V
VIN: to PGND (under steady-state conditions)	57 [2, 3]	V
GATE, VBIAS, VBP: to PGND	20	V
LDET: to VIN	no more than 6V less than VIN	V
ADCIN: to PGND	4	V
RB, VDD5I, TEST1, TEST2: to PGND	6	V
VDD3V_OUT, VDD3V_IN: to PGND	4	V
ISENSEP, CSS, SYNC_DLY, SYNC_OVL, MODE, GPIP, GPOP, PRI_DIV, I2C_ADR, SEC_DIV, WD_MODE: to PGND	4	V
VBOOST: to SGND	12	V
VP, LX2, LX3, LX4, LX4_SENSE, FB1, FB2, FB3, FB4: to SGND	6	V
CLK_IN, ISENSES, SEC_EN, COMP1, AGND1, PGOOD, VDD3V_ISEC, VDD3V_OSEC: to SGND	4	V
VDD_SYNC, SYNC_OUT, INTB/nc, SCL/GPIS, SDIO/GPOS, WDOG: to SGND	6	V
AGND2, AGND3, AGND4, COMP4, ISENP4, ISENN4, LSD4, HSD4, EN2, EN3, EN4, BUCK_EN: to SGND	6	V
ESD Rating, Human body model (per JESD22-A114)	2	kV
ESD charged device model	500	V
ESD machine model	200	V
ESD System level (contact/air) at RJ-45 (per IEC61000-4-2)	8/15	kV
Storage Temperature	165	°C
Operating Junction Temperature	125	°C

[1] The AS14x4 devices all have fast internal surge clamps for transient conditions such as system startup and other noise conditions; the devices must not be exposed to sustained over-voltage condition at this level.
[2] Under steady state conditions; higher voltage level is acceptable under transient conditions.
[3] See the Application Diagram (Figure 25) for device usage in designs requiring sustained input voltage > 57V.
Unless otherwise noted all Test Specifications apply over the full -40°C to 85°C operating temperature range.

Table 4 - Normal Operating Conditions

Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN	9.5		57[2]	V	
Thermal Resistance, Junction to Case, θ_{JC}		5		°C/W	
Thermal Resistance, Junction to Ambient, θ_{JA}		20		°C/W	
Operating temperature range	-40		85	°C	

[1] Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] See the Application Diagram (Figure 25) for device usage in designs requiring sustained input voltage > 57V.

Table 5 - Primary Side Digital, I/O, and A/D Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_OUT	Voltage from internally generated 3V source.	3.0	3.3	3.6	V	External bias-winding for VBIAS must be in use. Decouple VDD3V_OUT with 4.7µF cap. Referenced to PGND.
I_{VDD3V_OUT}	Current output from internally generated 3V source.			5	mA	
VDD3V_IN	3V primary side voltage input.	3.0	3.3	3.6	V	Supplied by VDD3_OUT, Referenced to PGND.
VDD5I	Voltage from internally generated 5V node.	4.0	5	6.0	V	Decouple with 1.5µF cap, referenced to PGND.
I_{VDD5I}	Current output from internally generated 5V node.			5	mA	
V_{HGPOP}	GPOP voltage output – high	3.0			V	Current at GPOP = 1.0 mA (VDD3V_IN=3.3V, referenced to PGND).

VLGPOP	GPOP voltage output – low			0.4	V	Current at GPOP = -1.0 mA (VDD3V_IN=3.3V, referenced to PGND).
VHGPIP	GPIP voltage input - high	2.0			V	(VDD3V_IN=3.3V, referenced to PGND).
VLGPIP	GPIP voltage input - low			0.8	V	(VDD3V_IN=3.3V, referenced to PGND).
TGPIO	Primary side GPIO pin latency to register update.			10[2]	ms	Independent of I²C clock speed. Pin I/O is automatic to and from I²C registers.
TADCIN	ADCIN pin latency to register update.			10[2]	ms	
VADCIN	ADCIN voltage range	0		2.5	V	Referenced to PGND.
RADCIN	ADCIN resolution			8	bits	
ADCERROR	ADCIN total unadjusted error			±TBD[3]	LSB	
ILADCIN	ADCIN input leakage current			100[2]	nA	
CADCIN	ADCIN input capacitance			0.3[2]	pF	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.
[3] Includes offset, full-scale, and linearity.

Table 6 - Primary Side DC-DC Controller Section Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VIN	Input voltage	9.5		57[4]	V	
VLDET_ON	Local input voltage threshold for Local Power Mode - ON	48VIN-2.4V			V	See Table 3 for Absolute Maximum Rating for LDET (referenced to PGND).
VLDET_OFF	Local input voltage threshold for Local Power Mode - OFF			48VIN-1.2V	V	
VBIAS	External bias source voltage	8[2]		14[2]	V	Sets VOH of GATE.
FPWM1L	Low end of Primary PWM switching frequency range		104		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 13.
FPWM1H	High end of Primary PWM switching frequency range		512		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 13.
FOSC1	PWM1 clock frequency accuracy	-20		+20	%	See Table 13 for frequency.
F1_MOD	PWM1 clock spread spectrum modulation		10		%	Factory default. Programmable in software capable devices (AS1454/34).
FPWM1T	PWM switching frequency temperature coefficient		0.12		%/C°	Refer to Table 13 for PWM Frequency.
RH_GATE	GATE drive impedance		6		Ω	High side output drive resistance, Source.
RL_GATE			6		Ω	Low side output drive resistance, Sink.
VPK1P	Peak current sense threshold voltage at ISENSEP		395		mV	Ipeak = VPK1P / RISENSEP.
DMAX1	Primary PWM Maximum duty cycle	80[3]			%	

DMIN1	Primary PWM Minimum duty cycle			10[3]	%	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by characterization. Not tested in production.
[3] Guaranteed by design. Not tested in production.
[4] See the Application Diagram (Figure 25) for device usage in designs requiring sustained input voltage > 57V.

Table 7 - Secondary Side Sync Controller (Output #1) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VSYNC_OUT	SYNC_OUT voltage	4.5	5	6	V	
RH_SYNC	SYNC_OUT Source Impedance VDD_SYNC = 5V			2.5	Ω	Source
RL_SYNC				2.5	Ω	Sink
VMR1	Output 1 voltage margining range		±5		%	Software mode, see Table 30.
VREF1	FB1 voltage reference	0.98	1.0	1.02	V	
ILEA1	Error amp leakage			1[2]	µA	
Gm1	Feedback Transconductance (Siemens)	150	225	350	µS	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 8 - Secondary Side DC-DC Regulators (Outputs #2, #3) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VP	Input Voltage at both VP pins	2.97		5.5	V	Nominally from Output #1
VOUT23_MIN	Output Voltage - Min		0.8		V	Application dependent, please see the Akros Design Guide, AN091, for addition information.
VOUT23_MAX	Output Voltage - Max		VP-0.7			
TEN23_DLY	External EN2/3 power-on delay (cap on the EN2/3 pin)	8[3]			ms	SEC_EN cap = 10nF (typical)
VEN23_ON	EN2/3 threshold – On	0.75	0.82	1.0	V	Low to high transition
VEN23H	EN2/3 hysteresis	100		200	mV	
FPWM23L	Low end of PWM2 / PWM3 switching frequency range		500		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins, see Table 13
FPWM23H	High end of PWM2 / PWM3 switching frequency range		2000		KHz	Set by external resistors on PRI_DIV and SEC_DIV pins see Table 13.
F23_MOD	PWM2 / PWM3 clock spread spectrum modulation		10		%	Factory default. Programmable in software capable devices (AS1454/34)
FOSC23	PWM2 / PWM3 clock frequency accuracy	-20		+20	%	See Table 13 for frequency.
DMAX23	PWM2 / PWM3 Maximum duty cycle	85[2]			%	
DMIN23	PWM2 / PWM3 Minimum duty cycle			10[3]	%	
IOUT23A	RMS Output Current AS1424/34	0		1.25[3]	A_{RMS}	AS1424/34 devices see note 2.
IOUT23B	RMS Output Current AS1444/54	0		2[3]	A_{RMS}	AS1444/54 devices see note 2.
RPFET23	P-Channel Rdson, #2 and #3 Outputs			180[3]	mΩ	VP = 5.0V
RNFET23	N-Channel Rdson, #2 and #3 Outputs			120[3]	mΩ	VP = 5.0V
LXLK23	LX2, LX3 Leakage Current		0.1	1[3]	µA	
LXLK23A	Output #2, #3 Current Limit AS1424/34	1.875[3]			A_{PEAK}	AS1424/34 devices see note 2.

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
LXLK23B	Output #2, #3 Current Limit AS1444/54	33			APEAK	AS1444/54 devices see note 2.
VMR23	Outputs #2, #3 voltage margining range		-8 / +6		%	Software mode, see Table 30 and Table 31.
VREF23	FB2 and FB3 Reference Voltage	784	800	816	mV	
ILFB23	FB2 and FB3 Leakage Current			0.23	µA	
IL_EN23	EN2/EN3 Leakage Current	9	10	11	µA	
IOFF23	#2 and #3 Regulator Shutdown Current		0.1	1.03	µA	EN2, EN3 in disable mode

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Maximum channel current is limited by the total combined power dissipation of all the DC-DC Regulators.
[3] Guaranteed by design. Not tested in production.

Table 9 - Secondary Side DC-DC Controller (Output 4) Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
$V_{OUT4\_MIN\_BUCK}$	Buck Output Voltage – Min		0.8		V	Application dependent, please see the Akros Design Guide, AN091, for addition information.
$V_{OUT4\_MAX\_BUCK}$	Buck Output Voltage – Max		VP-0.7		V	
$V_{OUT4\_MAX\_BOOST}$	Boost Output Voltage - Max		30V		V	
T_{EN4_DLY}	External EN4 power-on delay (cap on the EN4 pin)	8[2]			ms	SEC_EN cap = 10nF (typical)
V_{EN4_ON}	EN4 Threshold – On	0.75	0.82	1.0	V	Low to high transition
V_{EN4_H}	EN4 hysteresis	100		200	V	High to low transition
$V_{BUCK\_EN\_HI}$	BUCK_EN input voltage threshold - high	2.0			V	
$V_{BUCK\_EN\_LOW}$	BUCK_EN input voltage threshold - low			0.8	V	
F_{PWM4L}	Low end of PWM4 switching frequency range		125		KHz	1/4 of internal Buck frequency. Set by external resistors on PRI_DIV and SEC_DIV pins; see Table 13.
F_{PWM4H}	High end of PWM4 switching frequency range		500		KHz	
F4_MOD	PWM4 clock spread spectrum modulation		10		%	Factory default. Programmable in software capable devices (AS1454/34)
F_{OSC4}	PWM4 clock frequency accuracy	-20		+20	%	See Table 13 for frequency.
R_{H_HSD4}	HSD4 drive impedance		4		Ω	High side output drive resistance, Source
R_{L_HSD4}			4		Ω	High side output drive resistance, Sink
R_{H_LSD4}	LSD4 drive impedance		4		Ω	Low side output drive resistance, Source
R_{L_LSD4}			4		Ω	Low side output drive resistance, Sink
V_{PK4N}	Peak current sense threshold voltage at max load (ISENP4 – INSENN4)		60		mV	IL max
V_{PK4SS}	Peak current sense threshold		90		mV	current limit

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
	voltage at short circuit (ISENP4 – ISENN4)					(typically 50% above IL max)
DMAX4	PWM4 Maximum duty cycle	852			%	
DMIN4	PWM4 Minimum duty cycle			102	%	
VMR4	Output #4 Voltage Margining Range		-8 / +6		%	Software mode, see Table 30 and Table 31
VREF4	FB4 Reference Voltage	784	800	816	mV	
ILLX4	LX4 Leakage Current		0.1	12	µA	
ILFB4	FB4 Leakage Current			0.22	µA	
IL_EN4	EN4 Leakage Current	9	10	11	µA	
Gm4	Feedback Transconductance	50	78	95	µS	Units in µSiemens
IOFF4	#4 Controller Shutdown Current		0.1	1.02	µA	EN4 in disable mode

[1] Typical values at: Ta = 25°C, VP = 5VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 10 - Secondary Side Digital I/O and I²C Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
VDD3V_OSEC	Internally generated 3V source, referenced to SGND.	3.0	3.3	3.6	V	
IVDD3V_OSEC	VDD3V_OSEC current output (internally generated 3V source), referenced to SGND.			5	mA	TBD
VDD3V_ISEC	Power Supply Input Voltage	3.0	3.3	3.6	V	Sourced from VDD3V_OSEC
FCLK_IN	External Clock Input Frequency	23.75	25	26.25	MHz	
VCLK_IN_HI	CLK_IN input voltage threshold - high	2.0			V	
VCLK_IN_LOW	CLK_IN input voltage threshold - low			0.8	V	
IOINTB	INTB open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{INTB} (typ) = TBD
IOPG	PGOOD open drain current drive	1			mA	With $V_{PULL-UP}$ = TBD and $R_{PULL-UP}$ = TBDKΩ, V_{PGOOD} (typ) = TBD
TPGOOD	PGOOD minimum pulse output (High-Low-High)	10[2]			ms	
TWDOG	Watchdog minimum reset pulse width (WDOG pin)	100[2]			ns	
VHGPOS	GPOS voltage output – high (referenced to SGND)	3.0			V	Current at GPOS = 1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)
VLGPOS	GPOS voltage output – low (referenced to SGND)			0.4	V	Current at GPOS = -1.0 mA (VDD3V_ISEC=3.3V, referenced to SGND)

V_{HGPIS}	GPIS voltage input – high (referenced to SGND)	2.0			V	(referenced to SGND)
V_{LGPIS}	GPIS voltage input – low (referenced to SGND)			0.8	V	(referenced to SGND)
F_{SCL}	I^2C Clock Frequency	10		400	KHz	5V tolerant input
V_{IH}	I²C HIGH level input voltage	1.4			V	5V tolerant input
V_{ILI2C}	I²C LOW level input voltage			0.5	V	5V tolerant input
VOLI2C	I²C Output low voltage for pull-up voltage (VDD)			0.4		VDD > 2V, 2 mA sink
				0.2VDD		VDD < 2V, 2 mA sink
CDIO	Capacitance for each Digital I/O pin			102	pF	

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.
[2] Guaranteed by design. Not tested in production.

Table 11 - Thermal Protection Electrical Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit	Conditions
T_{SD}	Thermal shutdown temperature		140		°C	Above this temperature, the AS14x4 is disabled.
T_{I2C}	Thermal warning temperature for I^2C warning		115		°C	
T_{HYS}	Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

[1] Typical values at: Ta = 25°C, Vin = 48VDC. Typical specifications not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 12 - Isolation Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
I_{IO_ISO}	Input-output insulation			1.0[1]	µA	RH (Relative Humidity) = 45%, Ta = 25°C, t = 5s leakage current V_{IO_ISO} = 2250VDC (see note 1)
V_{ISO_DC}	Withstand insulation voltage DC	2120[1]			VDC	RH ≤ 50%, Ta = 25°C, t = 1min (see note 1)
V_{ISO_AC}	Withstand insulation voltage AC	1500[1]			V_{RMS}	RH ≤ 50%, Ta = 25°C, t = 1min (see note 1)
R_{IO_ISO}	Resistance (input to output)		TBD[1]	TBD[1]	Ω	V_{IO} = 250VDC (note 1)
CM	Common mode transient		10.0[2]		kV/µs	(see note 2)

[1] Device is considered a two terminal device: Primary pins are shorted together and Secondary pins are shorted together.
[2] All outputs to remain within ±3% tolerance during transient.

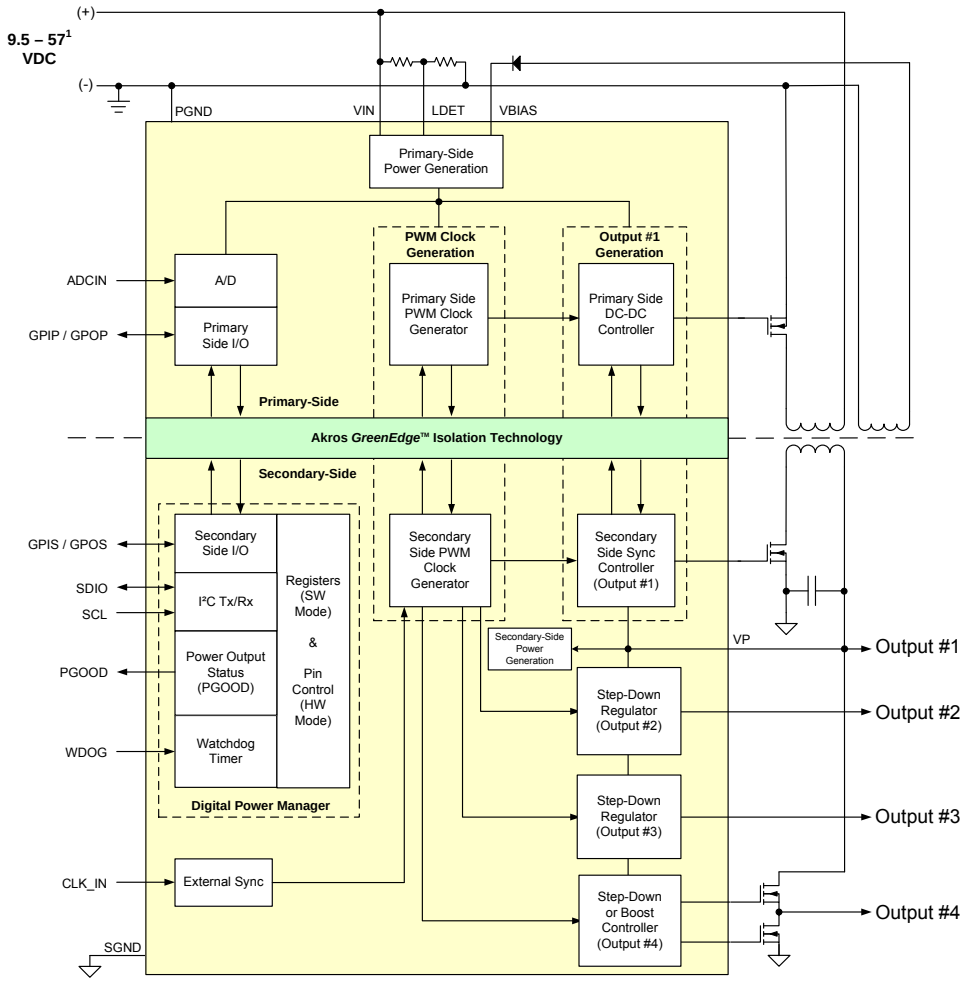
FUNCTIONAL DESCRIPTION

Figure 2 shows the block diagram of the as14x4. The individual blocks are described in greater detail in the following paragraphs (please also refer to these separate Akros documents for the as14x4: an091 for a detailed design guide and an092 for a detailed software user's guide).

ISOLATION

As shown in Figure 2 the AS14x4 is divided internally into Primary and Secondary sides. All signals that interconnect the Primary and Secondary sides are isolated using Akros *GreenEdge*™ technology eliminating the need for opto-isolators in both analog power control loop and the digital I²C paths between Primary and Secondary ground planes.

Figure 2 - AS14x4 Block Diagram



[1] See the Application Diagram (figure 25) for device usage in designs requiring sustained input voltage > 57V.

PWM Clock Generation

Figure 3 shows the AS14x4 PWM Clock Generation block diagram. During power-up, local oscillators on both sides of the isolation boundary provide separate clocks for Primary-side and Secondary-side PWMs. After power-up internal cross-isolation management automatically transitions all AS14x4 PWM clocks such that the Secondary-side oscillator becomes the master, and sources multi-phase clocks to both Primary and Secondary PWMs.

PWM Clock Frequency Configuration

Frequencies of all AS14x4 PWM clocks are set with resistors connected to the PRI_DIV and SEC_DIV pins as shown in Table 13.

External Clock Source (CLK_IN)

For additional EMI management, the CLK_IN pin provides an optional input for an external clock source to govern overall device timing. If used the local Secondary-side oscillator is slaved to CLK_IN, therefore Primary-side and Secondary-side PWM clocks are slaved to CLK_IN after power-up. The CLK_IN frequency should be 25MHz.

EMI Performance Control

A multi-phase clocking technique is used to generate clocks for the Primary DC-DC controller and all Outputs (1-4). This improves Electromagnetic (EM) radiation performance by reducing common mode noise and also reduces the size of external capacitors.

As an additional technique to reduce PWM clock induced harmonics in the power supplies, Fractional-N spread-spectrum modulation (set at 10%) is the default PWM clocking for all AS14x4 devices. In the AS1434 and AS1454 (software mode devices) modulation type, percentage, and usage can be user programmed via I²C register setup.

Figure 3 - PWM Clock Generation Block Diagram

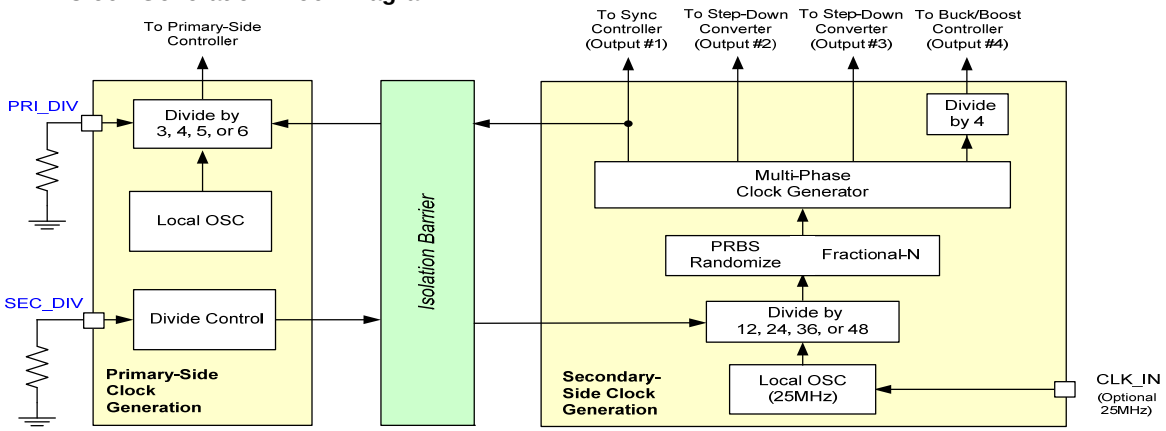


Table 13 - PWM Clock Rate Configuration

AS14x4 Master Clock Rate = Internal, or, 25MHz if using CLK_IN		PRI_DIV Resistor (Ω)			
		12.4K	43.2K	68.1K	100.0K
SEC_DIV Resistor (Ω)	Outputs #2/#3/#4 PWM Clock Rates (MHz)	PWM1 Clock Rate (KHz)			
12.4K	2.08 / 2.08 / 0.520	reserved	521	417	347
43.2K	1.04 / 1.04 / 0.260	347	260	208	174
68.1K	0.69 / 0.69 / 0.173	231	174	139	116
100.0K	0.52 / 0.52 / 0.130	174	130	104	reserved

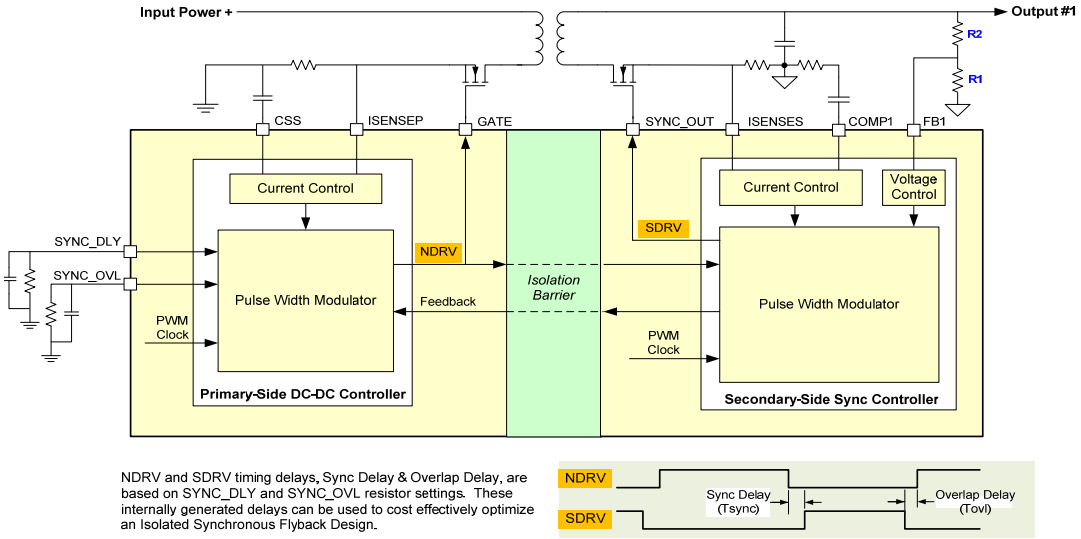
Power Output #1

Output #1 is the main AS14x4 power output and is typically used to supply the DC power that generates Outputs #2 thru #4.

As described in the previous section, the Primary and Secondary-side PWM clocks are generated and automatically synchronized across the integrated isolation barrier.

Figure 4 shows a typical synchronous Flyback design topology for Output #1.

Figure 4 - Power Output #1 Block Diagram



NDRV and SDRV timing delays, Sync Delay & Overlap Delay, are based on SYNC_DLY and SYNC_OVL resistor settings. These internally generated delays can be used to cost effectively optimize an Isolated Synchronous Flyback Design.

Three power control loop operations take place:

- Primary-side DC-DC controller FET driver switches the primary-side power FET from a loop error controlled PWM.
- Secondary-side sync controller FET driver switches the Secondary-side power FET to complete the Flyback power transfer cycle.
- The automated AS14x4 isolation management transmits Secondary-side loop feedback to the Primary-side PWM.

Typical isolated synchronous Flyback applications are shown in more detail in Figure 24 and Figure 25.

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Primary-side DC-DC Controller

The Primary-side DC-DC Controller is a current-mode DC-DC controller which is easily configured with a minimal set of external components. Isolation is provided by the internal Akros *GreenEdge*™ circuitry which eliminates the need for external opto-isolators.

The Primary-side DC-DC Controller includes: externally controlled soft start, 80% maximum duty cycle, fixed (after resistor programming) switching frequency and a true voltage output error amplifier.

Soft-Start Inrush Current Limit

Internal circuitry automatically controls the inrush current ramp by limiting the maximum current allowed in the transformer primary at startup. The amount of time required to perform this soft-start cycle is determined by a capacitor on the CSS pin. A CSS capacitor of 330nF provides approximately 7ms of soft startup ramp time.

Current-Limit and Current Sense

The primary side controller provides cycle-by-cycle current limiting to ensure the transformer primary current limits are not exceeded through use of an external resistor on ISENSEP. In addition, the maximum average current in the transformer primary is set by internal PWM duty cycle limits.

A short-circuit event is declared by the primary controller if this ISENSEP sensed current limit is triggered on more than 50% of the clock cycles within any 64 cycle window. Once a short-circuit event has been declared, Output #1 will shut off for 1024 cycles before a restart is attempted. This process will repeat indefinitely until the output short is removed.

Secondary-side Sync Controller

The efficiency of Output #1 can be optimized by designing a non-overlapping solution for the external FETs on the Primary side and Secondary side of the PD power transformer.

The FET sync and overlap delays, as shown in Figure 4, are controlled by the designer to compensate for rise, fall, and delay times for both Primary and Secondary-side external power FETs. See Table 14 and note the delay timing limit: (Tsync + Tovl) ≤ 25ns.

The required resistors at SYNC_DLY and SYNC_OVL to implement the desired Tsync and Tovl timing are then calculated; see an example in Table 15. Please also refer to the Akros application note AN091 for a detailed Design

Guide. The filter capacitors to SGND for these pins (see Figure 4) are 1nF, typical.

Table 14 - Sync & Overlap Delay Timing Limit

Sync Delay (ns)	Overlap Delay (ns)	Delay Timing Limit (ns)
Tsync	Tovl	(Tsync + Tovl) ≤ 25ns

Table 15 - SYNC_DLY & SYNC_OVL Resistor Calculation Example

Desired SYNC Delay (ns)	Desired Overlap Delay (ns)	Delay Timing Limit Check (ns)	SYNC_DLY Resistor Required (Ω)	SYNC_OVL Resistor Required (Ω)
Tsync	Tovl	(Tsync +Tovl) ≤ 25ns	R_{SYNC_DLY} = (Tsync + Tovl) x 2KΩ	R_{SYNC_OVL} = Tovl x 2KΩ
10ns	15ns	Ok	50KΩ	30KΩ

Compensation and Loop Feedback

The primary output (Output #1) has two power compensation and feedback mechanisms:

– Adaptive slope compensation

– Primary-Secondary control loop based feedback

The adaptive slope compensation automatically provides an optimized ramp framework for the overall loop performance, there are no user settings required.

For the Primary-Secondary control loop the device uses an internal transconductance error amplifier whose output compensates the control loop. An external secondary-side RC compensation network should be connecting to COMP1.

The resulting loop feedback path through the internal isolation channel to the primary-side PWM is automatic and completely user transparent.

Voltage feedback input is provided at the FB1 pin. At FB1, an internal reference of 1V (nominal) is compared to a resistor divided voltage from Output #1. This sets the desired Output #1 voltage level. With the top resistor in the feedback divider designated R2 and the bottom resistor designated R1 (again refer to Figure 4)
The programmed voltage for Output #1 is equal to Vref times (R1+R2)/R1. So, for example, with R1=5K, R2=20K, and Vref=1V, the output voltage is set to 5V.

Low-load Current Operation - DCM

The primary output (#1) uses both DCM and Pulse Skipping (Burst Mode) design techniques to optimize power efficiency. When a low-load output power condition is detected, the Controller automatically enters a discontinuous current mode (DCM) of operation.

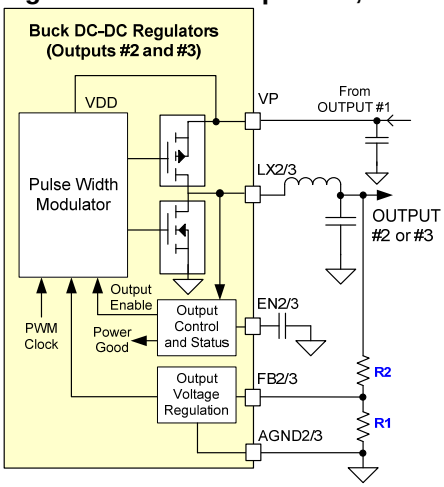
Over-voltage Protection

Output #1 has a built-in over-voltage monitor set to +10% of nominal voltage. If tripped, the output shuts down until within +5% of the nominal voltage at which point normal operation is then resumed.

If Voltage Margining is used, the over-voltage protection tracks to the margining selected.

Power Outputs #2 and #3

Figure 5 - Power Outputs #2, #3 Block Diagram



Secondary-side Outputs #2 and #3 (see Figure 5) are identical synchronous current mode PWM DC-DC Buck Regulators with:

– Integrated PMOS and NMOS Power FETs

– Independent low-noise remote ground sensing (AGND2, AGND3)

– Output drivers (LX2, LX3)

– Feedback voltage controls (FB2, FB3)

– Output power enable/sequencing (EN2, EN3)

Under normal operation the regulator uses the PWM to generate driver signals for internal high-side and low-side MOSFETs. To produce these PWM loop corrected outputs an error signal from the voltage-error amplifier is compared with a ramp signal generated by an oscillator in the PWM.

A high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. A low-side switch is then turned on for the remainder of the oscillator cycle.

Loop Feedback and Compensation

Voltage feedback is provided at the FBx (FB2 / FB3) pins. At FBx an internal reference of 800mV (nominal) is compared to a resistor divided voltage from the Output (#2/#3). This sets the desired Output voltage level, which is equal to Vref times (R1+R2)/R1.

Maximum voltage output level is constrained by the input level of VP: VOUT23 (max) = VP – 0.7V (typ).

Loop compensation is integrated for both Outputs.

Current-Limit and Current Sense

Each regulator provides cycle-by-cycle current limiting to ensure that the maximum current limits are not exceeded. For each PWM cycle during which the maximum current limit is tripped, a short-circuit counter is incremented. This counter is reset to zero if and only if two consecutive PWM cycles do not contain current limit events. If the counter reaches 16 a short-circuit event is declared and both Output #2 and Output #3 supplies are powered down. After 256 cycles of wait time both Outputs will attempt restarts. If the short-circuit persists the counter will begin to increment and the cycle will repeat itself.

Note that the internal Regulators for Output #2 and Output #3 are coupled together such that if one declares a short-circuit event they both reset regardless of the short-circuit counter status of the other.

Over-voltage Protection

Outputs #2/#3 each have built-in over-voltage monitors set to +10% of nominal voltage. If tripped the output is shut down until within +5% of nominal voltage, normal operation is then resumed.

If Voltage Margining is used, the over-voltage protection tracks to the margining selected.

Power Output #4

Secondary-side Output #4 is a synchronous current mode PWM DC-DC controller that drives external NMOS Power FETs and supports buck or boost topologies. Boost or buck operation is selected by the BUCK_EN pin.

Key Features:

- Independent low-noise remote sensing ground (AGND4)
- Current Sense inputs (ISENP4, ISENN4)
- High Side and Low Side NMOS FET drivers (HSD4, LSD4)
- DC-DC switch node output w/remote sense (LX4, LX4_SENSE)
- Feedback voltage control (FB4)
- Error amplifier compensation input (COMP4)
- Output power enable/sequencing input (EN4)
- PWM Dimmable LED Driver in Boost Mode

For typical Buck operation (Figure 6) the controller uses the PWM and generates driver signals for both high-side and low-side MOSFETs. To produce these PWM loop corrected outputs an error signal from the voltage-error amplifier is compared with a ramp signal generated by an oscillator in the PWM.

The external high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. The external low-side switch is then turned on for the remainder of the oscillator cycle.

For typical Boost operation (see Figure 7) the controller uses the PWM and generates only a low-side driver signal for a single external MOSFET. To produce this PWM loop corrected output an error signal from the voltage-error amplifier is compared with the ramp signal generated by an oscillator in the PWM.

The internal low-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the internally generated reference signal or the current-limit threshold is exceeded. The diode conducts for the remainder of the oscillator cycle.

Figure 6 - Power Output #4 Block Diagram - BUCK

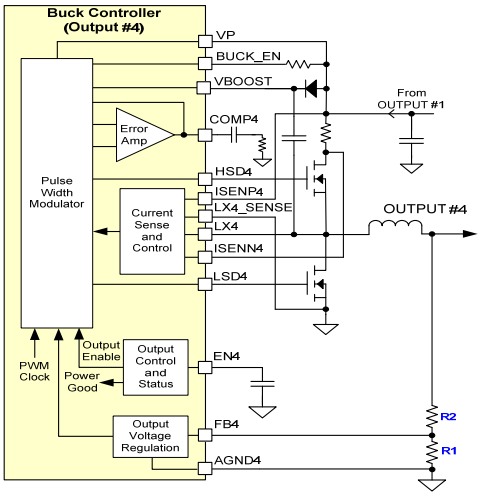
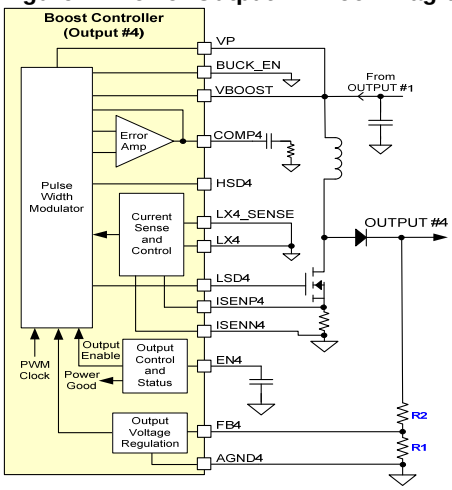
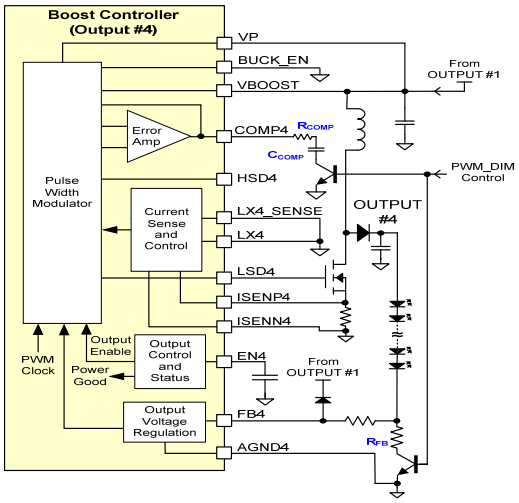


Figure 7 - Power Output #4 Block Diagram - BOOST



Extending the Boost mode to a PWM dimmable LED Driver (Figure 8) requires only the addition of external circuitry to hold the COMP4 and FB4 signal levels when the external PWM dim controller switches to dim (control on). The figure shows a low cost bipolar transistor solution, with an additional diode and resistor on FB4 to protect that input from LED string voltage during dimming.

Figure 8 - Power Output #4 Block Diagram - BOOST LED Driver



Compensation and Loop Feedback

As shown in Figure 6 and Figure 7 voltage feedback is provided at the FB4 pin in both Buck and Boost modes. At FB4 an internal reference of 800mV (nominal) is compared to a resistor divided voltage from Output #4 to control the voltage level. With the top resistor in the feedback divider designated R2 and the bottom resistor designated R1 the programmed voltage for Output #4 is equal to Vref times (R1+R2)/R1. So, in Boost mode operation, with R1=100, R2=1.43K, and Vref=0.8V, the output voltage is set to 12V.

In the LED Driver Boost application, Figure 8 in the R_{FB} resistor is used to keep a constant LED string current rather than a constant output voltage as was the case in the other (two resistor divider) control feedback loops described above. The other resistor in the feedback loop path now is connected directly to FB4 for enhanced pin protection from the LED string voltage during dimming. The diode to Output #1 is also for FB4 pin protection.

The COMP4 pin is connected to an external RC loop compensation network allowing design flexibility to optimize the system performance while insuring loop stability. In the LED Driver Boost application, again Figure 8, the compensation is held constant during dimming (control on) by the external transistor, and resumes compensation after PWM dimming control is removed (control off).

(Please refer to the AS14x4 Design Guide, AN091, for details).

Current-Limit and Current Sense

The Controller provides cycle-by-cycle current limiting to ensure that current limits are not exceeded, using an external resistor sensed at ISENP4 and ISENN4.

For each PWM cycle during which the maximum ISENP4-to-ISENN4 sensed current limit is tripped, a short-circuit counter is incremented. This counter is reset to zero if and only if two consecutive PWM cycles do not contain current limit events. If the counter reaches 16 a short-circuit event is declared and Output #4 is powered down. After 256 cycles of wait time Output #4 will attempt a restart, if the short-circuit persists the counter will begin to increment and the cycle will repeat itself.

Over-voltage Protection

Output #4 has a built-in over-voltage monitor set to +10% of nominal voltage. If tripped the output is shutdown until within +5% of nominal voltage, normal operation is then resumed.

If Voltage Margining is used (see Software Mode Operation) the over-voltage protection tracks to the margining selected.

HARDWARE MODE OPERATION

The Hardware mode of operation is designed to provide basic control and status of the device via hardware (pin) control signals. Hardware mode functions and operation are described below.

(Please also refer to the Akros document AN091 for a detailed Design Guide.)

Device Initialization & Hardware Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and PGND provides the power-on reset input required to initialize the device.

Hardware (HW) mode is selected when the MODE pin is also pulled-up High (in addition to the power-on reset capacitor to PGND). The VDD3V_OUT pin can be used for the MODE pin pull-up power source by using a 17.8KΩ (maximum) resistor from MODE to VDD3V_OUT.

Secondary-side digital logic is initialized while the SEC_EN pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset input required to initialize the secondary-side.

HW Mode Power Output Controls

Power Outputs #2 thru #4 each have independent output enable pins (EN2, EN3, and EN4) that enable the corresponding power output, and, can also be used to delay the power outputs relative to each other. Note that Output #1, the main device power output, is always enabled and does not have an output enable pin.

The ENx pins have internal pull-ups, so outputs are enabled when an ENx pin is simply connected to an external timing capacitor (C_{ENX}), see Figure 9.

As shown in Figure 10, a Low voltage (ground) on an ENx pin disables the corresponding power output. In addition, if an output is not used the associated FBx pin should in fact be pulled High to prevent a disabled output from affecting PGOOD status.

Figure 9 – HW Mode Output(s) Hardware Enabled

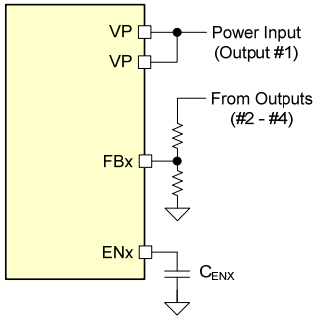
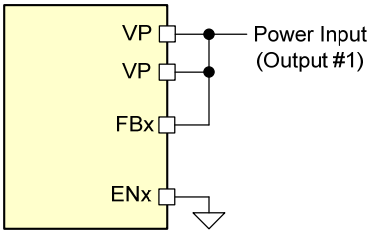


Figure 10 – HW Mode Output(s) Hardware Disabled



HW Mode Power Output Sequencing

Connecting a grounded external capacitor to an ENx pin establishes a delay before the corresponding power output is turned on. Each power output delay capacitor can be selected to create a user defined power-on sequence.

The time delay (T_{ENX}) in seconds for a capacitor (C_{ENX}) is defined by the formula:

$$T_{ENX} = \frac{0.8C_{ENX}}{10\mu A} \text{ (must be > 8ms)}$$

For example, a 200nF cap creates an output delay of 16ms. Each ENx pin has an internal 0.8V threshold detector and sources 10µA. When the ENx pin reaches 0.8V, enable delay timing begins.

Each ENx delay must be greater than 8ms for proper device startup assuming a typical 10nF capacitor on SEC_EN. All delays for power outputs #2-#4 are synchronized to the beginning of the Output #1 voltage ramp (see Figure 11).

Figure 11 – HW Mode Power Output Sequencing Example

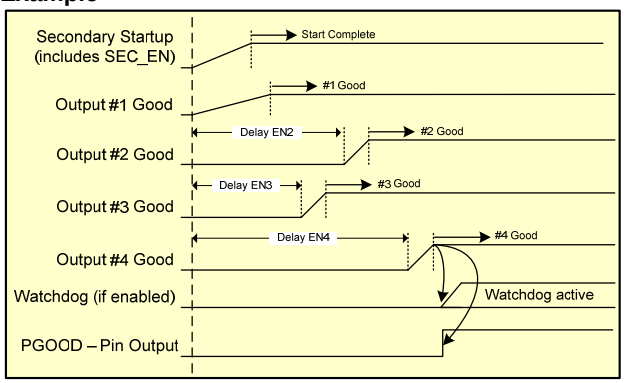
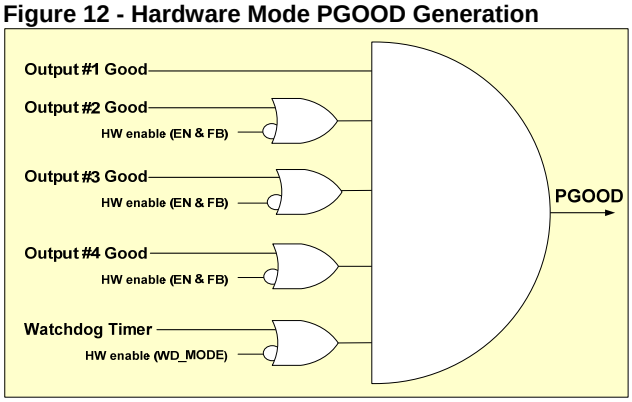


Figure 12 - Hardware Mode PGOOD Generation



HW Mode Power Monitoring (PGOOD)

All Outputs (1-4) are monitored for power good status if enabled (2-4 can be disabled). Once a supply output reaches a stable state, its internal power good status signal is asserted. An output's power good is declared (good) at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either transition case (good to/from bad), continuous operation of 10µS is required before the state change is declared. The user sees the resulting status on the PGOOD pin (10ms minimum pulse).

In Hardware mode, the PGOOD pin is the logical AND of all enabled Power Outputs and any Watchdog timeout events (if enabled) as shown in Figure 12.

If any of power outputs (2-4) are not required, the unused output(s) should be permanently disabled using the ENx and FBx pins as described in HW Mode Power Output Controls. Permanently disabling an unused output is required to assure correct PGOOD signal "ANDing".

HW Mode Watchdog Timer

Watchdog Configuration

The Watchdog timer is configured by the WD_MODE pin as follows:

– When the WD_MODE pin is set High the Watchdog timer is set for a 32 second timeout period.
– When the WD_MODE pin is Floating the Watchdog timer is set for a 1 second timeout period. Decoupling the pin to PGND is also required.
– When the WD_MODE pin is set Low the Watchdog timer function is disabled.

Watchdog Service

The Watchdog timer is serviced by pulsing the WDOG pin for at least 100ns (here a pulse is defined as a continuous level of either polarity after the 1st edge). Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout

If the Watchdog times out, the following occur:

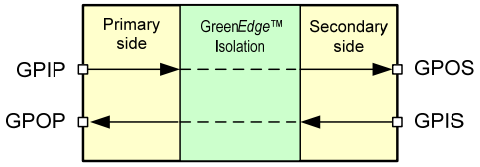
– The PGOOD pin is pulsed Low for 10ms (min). If coincident with any voltage fault events the PGOOD output pulse could be longer. This pulse can be used for PD platform level alarm or reset.
– Operation of the Watchdog timer is automatically initialized and restarted.

HW Mode General-Purpose I/O Operation

In Hardware mode, the GPIO pins provide a means for controlling and monitoring isolated primary-side signals from the secondary-side of the AS14x4.

The secondary-side GPOS and GPIS pins map to the primary-side pins GPIP and GPOP as shown in Figure 13.

Figure 13 - Hardware Mode GPIO Pin Mapping



SOFTWARE MODE OPERATION

Software mode operation allows a host controller to access the AS1454/34 internal registers via an I^2C interface. Access to these registers provides extensive status and control functions. Software mode functions and operation details are described below.

(Please also refer to the Akros document AN092 for a detailed Software Users Guide.)

Device Initialization and Software Mode Selection

Primary-side digital logic is initialized while the MODE pin is Low, A required external capacitor between MODE and PGND provides the power-on reset input required to initialize the device.

Software (SW) mode is selected when the MODE pin uses just this initialization capacitor.

Secondary-side digital logic is initialized while the SEC_EN pin is Low, a required external capacitor between SEC_EN and SGND will provide the power-on reset required to initialize the secondary-side.

SW Mode Power Output Controls

Once enabled in hardware, Power Outputs (2-4) can be independently enabled or disabled in both Hardware (via pin control) and Software (via I²C register).

Each output has an independent enable pin (EN2, EN3, EN4) for hardware enabling, and, can also be used to delay one voltage output relative to other. Note that Output #1, the main device power output, is always enabled and does not have an output enable pin or software control mode.

Any power output (2-4) to be software controlled must first have been enabled in hardware. The ENx pins have internal pull-ups, so outputs are enabled when an ENx pin is simply connected to an external timing capacitor (C_{ENX}), see Figure 14.

As shown in Figure 15, a Low voltage (ground) on an ENx pin disables the corresponding power output; any hardware disabled output will not be controllable in software. In addition, if an output is not used the associated FBx pin should in fact be pulled High to prevent a disabled output from affecting PGOOD status.

Figure 14 – SW Mode Output(s) Hardware Enabled

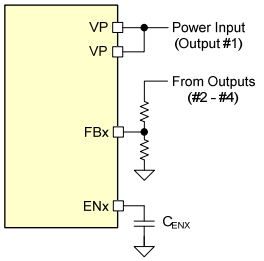
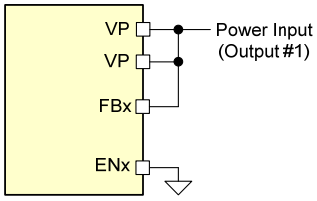


Figure 15 – SW Mode Output(s) Hardware Disabled



SW Mode Power Output Sequencing

Connecting a grounded external capacitor to an ENx pin establishes a delay before the corresponding power output is turned on. Each power output delay capacitor can be selected to create a user defined power-on sequence.

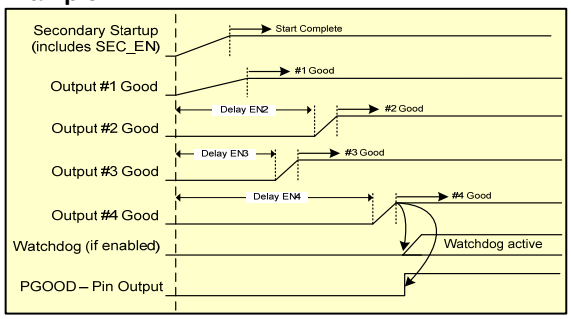
The time delay (T_{ENX}) in seconds for a capacitor (C_{ENX}) is defined by the formula:

$$T_{ENX} = \frac{0.8C_{ENX}}{10\mu A} \quad \text{(must be > 8ms)}$$

For example, a 200nF cap creates an output delay of 16ms. Each ENx pin has an internal 0.8V threshold detector and sources 10µA. When the ENx pin reaches 0.8V, enable delay timing begins.

Each ENx delay must be greater than 8ms for proper device startup assuming a typical 10nF capacitor on SEC_EN. All delays for power outputs (2-4) are synchronized to the beginning of the Output #1 voltage ramp see Figure 16.

Figure 16 – SW Mode Power Output Sequencing Example



SW Mode Power Status Monitoring (PGOOD)

Each power output (1-4) is monitored for power good status. Once a supply output reaches a stable state its internal power good status signal is asserted. An output's power status is declared good at +/- 5% and at fault (bad) at +/- 10% of final voltage value. In either

transition case (good to/from bad) a continuous operation of 10µS is required before state change is declared.

As shown in Figure 17, once all enabled outputs are good the user will see the resulting device power status on both the PGOOD pin and the Global PGOOD bit of Register 00h.

Power Good status for each supply is available in the Alarms and Power Status register (00h).

Operation of the PGOOD pin is defined by register 03h as shown in Table 22. Register 03h allows the user to exclude any individual output's power good status from affecting the PGOOD pin by clearing the associated output's mask bit. If the default values in register 03h are used, PGOOD is the logical AND of all four power status outputs. As shown in Figure 17, a fault on any of the supplies will drive the PGOOD pin Low (10ms minimum).

In addition, the Watchdog timer status can be included / excluded in the PGOOD pin logic. Register 04h, bit 2 allows the user to either mask or allow a Watchdog timeout to generate a PGOOD pulse.

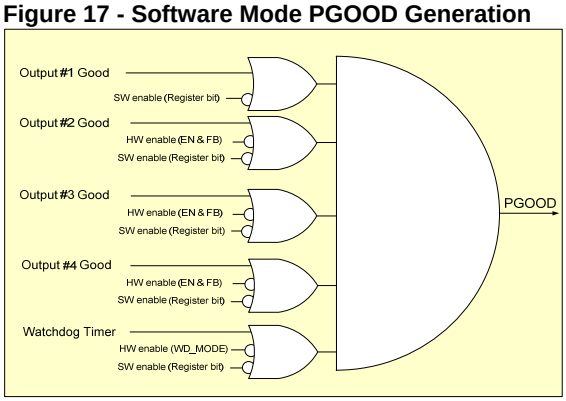
The PGOOD pin can be used as part of a board reset logic chain as it is asserted (High) only when all the enabled power outputs are stable.

If any of power outputs (2-4) are not required, the unused output(s) should be permanently disabled using ENx and FBx pins.

Permanently disabling an output will override any register control associated with a disabled output.

Power voltage monitoring will not restart any of the supplies. Also, a PGOOD fault will restore all registers except the history register (Reg 05h) to default state unless bit 4 in the device control register (Reg 06h) is set.

Figure 17 - Software Mode PGOOD Generation



History Register

The PGOOD & Watchdog History register (05h) is used to identify the source of a PGOOD fault. One bit is provided for each power output (1-4) and one for the Watchdog timer. In the event of a PGOOD fault, the bit corresponding to the particular power output that caused the PGOOD fault is set. Similarly, in the event of a Watchdog timeout the Watchdog Timeout bit is set.

Once set these bits are latched, they will not change even after the PGOOD fault is resolved unless there is a user command to do so. Therefore the user must clear this register as desired. The PGOOD & Watchdog History register is described in Table 24.

SW Mode Power Margining

Each of the four voltage outputs can be independently margined. Output #1 has a margining range of -5% to +5%; the other Outputs (2-4) can be independently margined from -8% to +6%.

These are configured via the Margin Control registers 0Eh and 0Fh. This feature allows engineering and/or manufacturing testing where, for example, it is useful to make test adjustments to compensate for PC board trace IR drops. See Table 30 and 31 for details.

If voltage margining is used in the AS1434 or AS1454, over-voltage protection tracks to the margining selected for any output.

SW Mode EMI Performance Control

As an additional technique to reduce PWM clock induced harmonics in the power supplies, Fractional-N spread-spectrum modulation (set at 10%) is the default PWM clocking for all AS14x4 devices. In the AS1434 and AS1454 Software mode devices modulation type, percentage, and usage can be user programmed via I²C register setup.

The AS1454 and AS1434 provide two user controlled methods to generate PWM spread-spectrum clocks for optimum EM radiation performance: PRBS Randomization and Fractional-N.

PWM Clocks - PRBS Randomization

This technique enables a randomized PRBS sequence to modulate the clocks thus spreading the noise across the band and reducing the peaks. PRBS randomization is selected via register 0Ah as shown in Table 29.

PWM Clocks - Fractional-N

Fractional-N clocking provides an “FM like” modulation on the PWM clocks that spreads out the spectral energy thereby reducing peaks in EMI tested frequency bands. One of three modulation rates for this technique can be selected via register 0Ah as shown in Table 29.

SW Mode General-Purpose I/O & ADC

As shown in Figure 18, the GPOP, GPIP, and ADCIN pins provide a means for controlling and monitoring isolated Primary-side signals from the Secondary side of the AS1454/34. GPIO and A/D functions are updated automatically at a 100Hz (minimum) rate, and may be accessed at any valid I²C clock rate.

General-Purpose I/O Pins

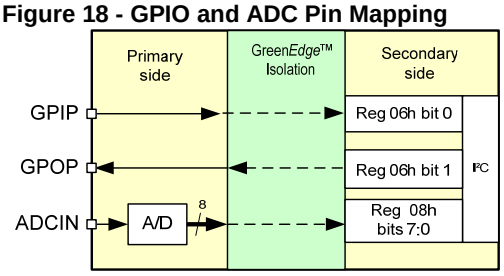
The GPOP bit in the Device Control register (06h) specifies the state of the GPOP output pin. The state of GPIP input pin is reflected in GPIP bit located in the same register. Maximum measurement latency is defined in Table 5.

General-Purpose ADC (ADCIN Pin)

The Primary-side ADCIN pin is an input to an internal A/D converter with a continuous sample/conversion rate. The A/D process is automatic and therefore requires no user action to initiate. This internal 8-bit A/D sub-system contains a successive approximation A/D, track/hold circuitry, internal voltage reference, and conversion clocking. Reading the converted value is done in the A/D Voltage register (08h). Maximum measurement latency is found in Table 5.

In addition, the A/D Alarm Threshold register (09h) allows the user to specify a maximum A/D value that when exceeded automatically sets the A/D Over-threshold Alarm bit in register 00h.

Figure 18 - GPIO and ADC Pin Mapping



SW Mode Watchdog Timer Operation

The Watchdog timer is serviced using either the WDOG pin or the Watchdog Service Control bit in Register 04h. Correct platform usage is to service before the watchdog timeout occurs.

If a Watchdog timeout occurs, the PGOOD pin can generate an output pulse (10ms minimum) that may be used for PD platform level alarm or reset. In addition, an interrupt can be generated and the status can be interrogated by querying the Interrupt Status register (02h) which has a bit to indicate Watchdog timeout.

Watchdog Timer Modes

In Software mode (MODE pin Floating with cap to PGND), the WD_MODE pin selects one of three Watchdog timer operating modes as follows:

Watchdog Timer Function Disabled

When the WD_MODE pin is set Low, the Watchdog timer function is disabled.

Watchdog Timer Enabled at Startup

When the WD_MODE pin is connected to an external capacitor (to PGND), the watchdog timer function is enabled at startup. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Disabled at Startup

Setting the WD_MODE pin High disables the Watchdog timer function at startup and can only be enabled through software. At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. Once the Watchdog is enabled the timeout period may be changed via the Watchdog Timeout register (07h) as described below.

Watchdog Timer Operation

Watchdog Enable

Enabling of the watchdog function in software must be done with two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit "Enable Watchdog", plus any other Watchdog bit masks (for Interrupts, PGOOD, and Register Reset functionality).

2. The next write must be to register 00h with the value BBh with no other intervening read or write operation to the AS1454/34. The time between the two writes can be infinite, but the operation will not be enabled until the second write. If a write/read occurs to any other register or if a write occurs but the value is NOT BBh, the Enable Watchdog bit is cleared.

Note that once enabled, watchdog operation cannot be disabled.

Watchdog Service

To service the watchdog via software, the user must issue two consecutive writes as follows:

1. The first write is to the Watchdog register (04h) bit "Watchdog Service Control".

2. The next write must be to register 00h with value AAh with no other intervening read or write operation to the AS1454/34. The time between the two writes can vary; however, the second write must be completed before a watchdog timeout occurs. If the watchdog times out before the second write or the second write is not to the 00h register or the data value is not "AAh", then the service request to the watchdog timer is cancelled.

To service the watchdog via hardware (a valid operation in Software mode) the WDOG pin must be pulsed for at least 100ns (continuous pulse of either polarity after the 1st edge). Correct platform usage is to service before the watchdog timeout period expires.

Watchdog Timeout Period

At startup the watchdog timeout counter defaults to the maximum period of 32 seconds. The current user programmed value in the Watchdog Timeout register (07h) is always used for watchdog timeouts. A value of FFh in this register gives the maximum timeout of 32 seconds. A value 01h sets the minimum period of 125ms. Note that 00h is reserved and is not to be used. Intervening values are multiples of 125ms (e.g. a value of 04h = 500ms).

Watchdog Timeout

If the Watchdog times out, the following occur:

– The Watchdog Timeout bit in the History register (05h) is set.

– If the Watchdog Interrupt mask bit is set (register 04h) and interrupts are enabled, the Watchdog Timeout bit in the Interrupt Status register (02h) is set and the INTB pin is driven Low.

– If the Watchdog PGOOD mask bit is set (register 04h), a 10ms (min.) Low pulse is output at the PGOOD pin. If coincident with other voltage fault events the PGOOD output pulse could be extended.

– If the Watchdog Register Reset mask bit is NOT set (register 04h), the AS1454/34 registers are reset. This resets the Watchdog Timeout register value to 32 seconds. (Note that an independent PGOOD fault will also reset the registers unless bit 4 in device control register, Reg 06h, is set).

– If the Watchdog Register Reset mask bit is set (register 04h), operation of the Watchdog timer is automatically initialized, with the currently programmed value, and restarted.

SW Mode Interrupt Operation

Interrupts are disabled after a device power on. The Device Control register (06h) is used to enable (or disable) interrupts at a global device level.

The Interrupt Mask (01h) and Interrupt Status (02h) registers are used to enable alarms and service any resulting alarms.

Interrupt Masking

Positive masking is used; therefore a "1" indicates that the specified fault or alarm will cause an interrupt. Interrupts (except for watchdog timeout) are level-driven, thus if a fault condition is active upon enabling it will immediately generate an interrupt.

Interrupt Status

A read from the Interrupt Status register will return the conditions which have caused an interrupt, and will immediately clear all such pending interrupts. Note that interrupts (except for watchdog timeout) are level driven, so if a fault condition still exists upon interrupts being cleared an interrupt will be re-asserted after a minimum off time of 10µs.

I^2C Interface

The AS1454/34 provides a standard I^2C compatible slave interface that allows a host controller (master) to access its single-byte registers. Note the requirement of "Repeated Start" for I^2C reads.

The Primary-side GPIO pin read/write or ADCIN pin conversion read/write have a 10ms (maximum) pin-to/from-register timing.

The AS1454/34 registers are summarized in Table 18 and described in Table 19 through Table 31.

The I^2C interface is active when the AS1454/34 is in Software mode. There are four pins associated with the I^2C interface:

– SDIO: bi-directional serial data
– SCL: clock input
– INTB: interrupt output
– I2C_ADR: device address configuration

Start/Stop Timing

The master device initiates and terminates all I^2C interface operations by asserting Start and Stop conditions respectively.

As shown in Figure 19, a START condition is specified when the SDIO line transitions from High-to-Low while the clock (SCL) is High. A STOP condition is specified when SDIO transitions from Low-to-High while SCL is High.

Data Timing

As shown in Figure 19, data on the SDIO line may change only when SCL is Low and must remain stable during the High period of SCL. All address and data words are serially transmitted as 8-bit words with the MSB sent first.

Acknowledge (ACK)

ACK and NACK are generated by the addressed device that receives data on SDIO. After each byte is transmitted, the receiving interface sends back an ACK to indicate the byte was received. As shown in Figure 20, to generate an ACK, the transmitter first releases the SDIO line (High) during the Low period of the ACK clock cycle. The receiver then pulls the SDIO line Low during the High period of the clock cycle.

A NACK occurs when the receiver does NOT pull the SDIO line Low during the High period of the clock cycle.

Device address/operation words, register address words, and write data words are transmitted by the master and are acknowledged by the AS1454/34. Read data words transmitted by the device are also acknowledged by the master.

Figure 19 - I²C Interface Start/Stop and Data Timing

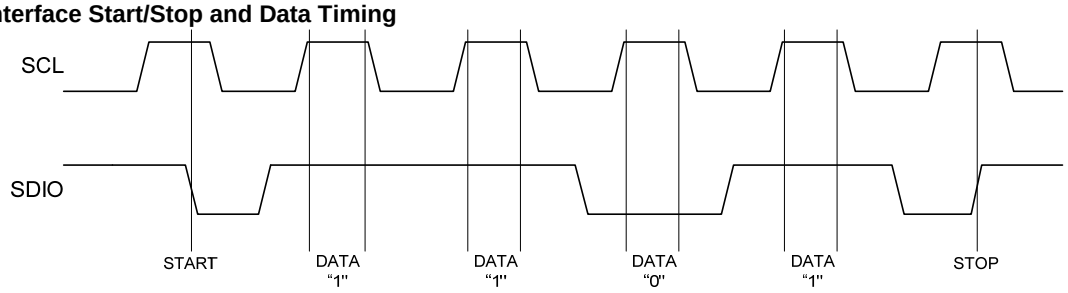
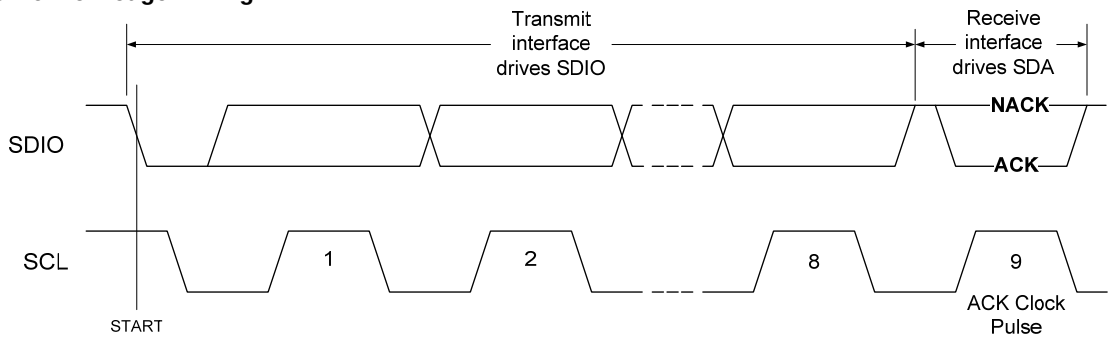


Figure 20 - I²C Acknowledge Timing



Device Address Configuration

The I²C interface is designed to support a multi-device bus system. At the start of an I²C read or write operation, the AS1454/34 compares its configured device address to the address sent by the master. The AS1454/34 will only respond (with ACK) when the addresses match.

The device address consists of 7 bits plus a read/write bit. As shown in
Table 16, bits A7, A6, A5 and A4 of the AS1454/34 device address are internally fixed to values A7 = 0, A6 = 1, A5 = 0 and A4 = 0.

The I2C_ADR pin is used to configure bits A3 thru A1 (using an external resistor). The device establishes the bit values of A3 thru A1 during start-up by measuring current flow through this resistor.
Note that A0 functions as the read/write operation bit.

Table 16 - AS1454/34 Device Address Configuration

Bit	Function	Description
A7	Fixed device address bits	Internally fixed to 0
A6		Internally fixed to 1
A5		Internally fixed to 0
A4		Internally fixed to 0
A3 A2 A1	Configurable device address bits	Device address bits A3, A2 and A1 are configured by connecting a 1% resistor between pin I2C_ADR and ground (PGND) as follows: 100KΩ□ sets A3, A2, A1 = 1,1,1 86.6KΩ□sets A3, A2, A1 = 1,1,0 75.0KΩ□sets A3, A2, A1 = 1,0,1 61.9KΩ□sets A3, A2, A1 = 1,0,0 49.9KΩ□sets A3, A2, A1 = 0,1,1 37.4KΩ□sets A3, A2, A1 = 0,1,0 29.4KΩ□sets A3, A2, A1 = 0,0,1 12.4KΩ□sets A3, A2, A1 = 0,0,0
A0	$R/\overline{W}$	Specifies read or write operation

Device Address/Operation Word

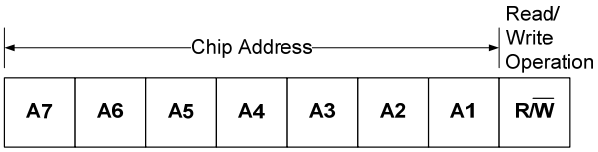
Following a START condition the host transmits an 8-bit device address/operation word to initiate a read or write operation. This word consists of a 7-bit device address and the read/write operation bit as shown in Figure 12.

The AS1454/34 compares the received device address with its configured device address and sends back an ACK only

when the addresses match.

Bit A0 is the read/write operation bit. A read operation is specified when the $R/\overline{W}$ bit is set High; a write operation when set Low.

Figure 21 - Device Address/Operation Word



Register Address Word

For write operations (after the AS1454/34 acknowledges receipt of the Device Address/Write Word) the master sends the target 8-bit register address word to specify the AS1454/34 register to be accessed. Table 17 specifies the valid AS1454/34 register addresses.

Data Word

The 8-bit data word contains read/write data. Data is transferred with the MSB sent first.

Write Cycle

Figure 22 illustrates the sequence of operations to perform an AS1454/34 register write cycle.

Read Cycle

Figure 23 illustrates the sequence of operations to perform an AS1454/34 register read cycle. Note that the master must first perform a “dummy write” operation to write the AS1454/34 internal address pointer to the target register address.

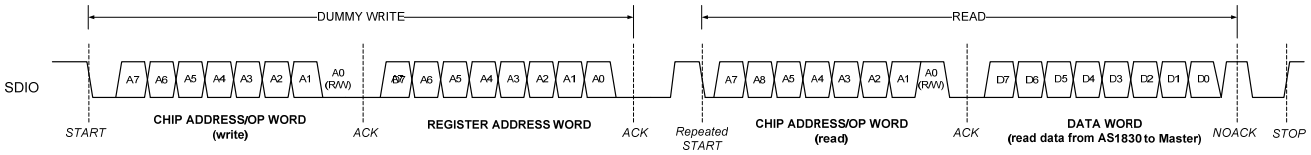
After the AS1454/34 sends back an ACK, the master sends a repeated START, followed by a device address read word ($R/\overline{W}$ bit = 1). The AS1454/34 then transmits an ACK followed by the data word that reflects the contents of the target register. Upon receipt of the register address word, the AS1454/34 sends back an ACK.

Table 17 - AS1454/34 Register Address Word

I^2C Register Address Word								Selected AS1454/34 Register (Hex)
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
0	0	0	0	0	0	1	0	02
0	0	0	0	0	0	1	1	03
0	0	0	0	0	1	0	0	04
0	0	0	0	0	1	0	1	05
0	0	0	0	0	1	1	0	06
0	0	0	0	0	1	1	1	07
0	0	0	0	1	0	0	0	08
0	0	0	0	1	0	0	1	09
0	0	0	0	1	0	1	0	0A
0	0	0	0	1	0	1	1	0B
0	0	0	0	1	1	0	0	0C
0	0	0	0	1	1	0	1	0D
0	0	0	0	1	1	1	0	0E
0	0	0	0	1	1	1	1	0F

Figure 22 - I²C Interface Write Cycle Timing

Figure 23 - I²C Interface Read Cycle Timing (with Repeated Start)



REGISTER DESCRIPTIONS

The AS1454/34 contains 16 single byte (8-bit) registers. The registers are accessible via the I²C interface when Software mode is enabled.

Table 18 provides a summary of AS1454/34 registers and bit map.
Table 19 through Table 31 provides detailed description of the function and operation of each register.

Table 18 - AS1454/34 Register and Bit Summary[1]

Register	Addr (hex)	Access	Data Bits D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask	01	R/W	reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	reserved
Interrupt Status	02	Read-Only	reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Watchdog Timeout
PGOOD Voltage Masks	03	R/W	reserved	reserved	reserved	Output #4 Mask	Output #3 Mask	Output #2 Mask	Output #1 Mask	reserved
Watchdog Enable, Mask, Service	04	R/W	reserved	reserved	reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	reserved	reserved	reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Timeout elapsed
Device Control and I/O Status	06	R/W	reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	reserved	reserved	GPOP	GPIP
Watchdog Timeout	07	R/W	WDOG timeout counter (8 bits, in 125ms increments)							
ADCIN Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
ADCIN Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							
System Clock Control	0A	R/W	reserved	reserved	reserved	reserved	PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	
Outputs 1,2 Disable & Margin Control	0E	R/W	Output #2 Disable Control	Output #2 Voltage Margin setting (D6, D5, D4)			reserved	Output #1 Voltage Margin setting (D2, D1, D0)		
Outputs 3,4 Disable & Margin Control	0F	R/W	Output #4 Disable Control	Output #4 Voltage Margin setting (D6, D5, D4)			Output #3 Disable Control	Output #3 Voltage Margin setting (D2, D1, D0)		

[1] In addition to the "reserved" register bits shown, registers 0B-0D(hex) are also reserved and should not be used.

Table 19 - Alarms and Power Status (Read-Only) - 00h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	Internal Over-temp Alarm	1 = Temp has tripped warning Threshold 0 = No alarm	0
D5	A/D Threshold Alarm	1 = A/D measurement is > A/D Alarm Threshold register setting 0 = No alarm	0
D4	Power Output #4 Fault	1 = Output #4 Fault, not within spec 0 = Output in spec	0
D3	Power Output #3 Fault	1 = Output #3 Fault, not within spec 0 = Output in spec	0
D2	Power Output #2 Fault	1 = Output #2 Fault, not within spec 0 = Output in spec	0
D1	Power Output #1 Fault	1 = Output #1 Fault, not within spec 0 = Output in spec	0
D0	Global PGOOD Fault	1 = At least one enabled output not within spec 0 = All enabled outputs within spec	0

Table 20 - Interrupt Mask (R/W) - 01h

Bit	Function	Description (see also Alarms and Power Reg)	Reset State
D7	reserved	do not write to this data bit	0
D6	Internal Over-temp Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D5	A/D Threshold Alarm	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D4	Interrupt upon Power Output #4 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D3	Interrupt upon Power Output #3 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D2	Interrupt upon Power Output #2 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D1	Interrupt upon Power Output #1 Fault	1 = mask on (interrupt possible) 0 = masked off (no interrupt possible)	0
D0	reserved	do not write to this data bit	0

Table 21 - Interrupt Status (Read-Only) - 02h

Bit	Function	Description (see also Alarms and Power Reg)	Reset State
D7	reserved	do not write to this data bit	0
D6	Internal Over-temp Alarm	1 = Fault 0 = normal operation	0
D5	A/D Threshold Alarm	1 = Fault 0 = normal operation	0
D4	Power Output #4 Fault	1 = Fault 0 = normal operation	0
D3	Power Output #3 Fault	1 = Fault 0 = normal operation	0
D2	Power Output #2 Fault	1 = Fault 0 = normal operation	0
D1	Power Output #1 Fault	1 = Fault 0 = normal operation	0
D0	Watchdog Timeout	1 = Timeout 0 = no timeout	0

Table 22 - PGOOD Voltage Masks (R/W) - 03h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Output #4 masked from PGOOD pin	1= Output #4 part of PGOOD pin or register status 0= Output #4 not part of PGOOD	1
D3	Output #3 masked from PGOOD pin	1= Output #3 part of PGOOD pin or register status 0= Output #3 not part of PGOOD	1
D2	Output #2 masked from PGOOD pin	1= Output #2 part of PGOOD pin or register status 0= Output #2 not part of PGOOD	1
D1	Output #1 masked from PGOOD pin	1= Output #1 part of PGOOD pin or register status 0= Output #1 not part of PGOOD	1
D0	reserved	do not write to this data bit	0

Table 23 - Watchdog Enable, Mask, Service (R/W) - 04h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Watchdog Enable	To change D4, D3, D2, or D1 a two stage write operation must occur: Stage 1. The Watchdog Enable bit (D4) must be set along with any other (D3-D1) desired bit changes. If D4 is not set the entire write operation is ignored. Stage 2. A write to Reg 0 with data BB (hex) must be the next I^2C operation to this device. If not, write will be ignored. Once this operation is complete (and D4 is set) the D4-D1 bits are sticky and cannot be reset. **D4 (Watchdog Enable):** 1 = enable watchdog countdown operation (timeout value set in watchdog timeout register). 0 = watchdog disabled **D3 (Watchdog Interrupt Mask):** 1 = mask on, interrupt possible 0 = masked off, no interrupt possible **D2 (Watchdog PGOOD Mask):** 1 = mask on, Watchdog part of PGOOD operation 0 = mask off, Watchdog not part of PGOOD operation **D1 (Watchdog Register Reset Disable Mask):** 1 = mask on, a Watchdog timeout will not reset I^2C registers 0= mask off, a Watchdog timeout will reset I^2C registers	D4 = 0
D3	Watchdog Interrupt Mask		D3 = 0
D2	Watchdog PGOOD Mask		D2 = 1
D1	Watchdog Register Reset Mask		D1 = 0
D0	Watchdog Service Control	1 = enable software service of Watchdog 0 = no software service of Watchdog Servicing the Watchdog is a 2-step procedure, after writing a "1" to this bit the next I^2C operation to the AS1454/34 must be a write to Reg 0 with data AA (hex).	0

Table 24 - PGOOD & Watchdog History (R/W) - 05h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	Output #4 PGOOD history	1 = Output #4 caused PGOOD fault 0 = Output #4 did not cause PGOOD fault	0
D3	Output #3 PGOOD history	1 = Output #3 caused PGOOD fault 0 = Output #3 did not cause PGOOD fault	0
D2	Output #2 PGOOD history	1 = Output #2 caused PGOOD fault 0 = Output #2 did not cause PGOOD fault	0
D1	Output #1 PGOOD history	1 = Output #1 caused PGOOD fault 0 = Output #1 did not cause PGOOD fault	0
D0	Watchdog history	1 = Watchdog timeout occurred 0 = No Watchdog timeout occurred	0

Table 25 - Device Control and I/O Status (R/W) - 06h

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	Reset all registers	1 = force reset all registers 0 = no resets	0
D5	Enable Interrupts	1 = enable interrupts that are masked on 0 = no interrupts enabled	0
D4	Disable PGOOD reset	1 = PGOOD fault will not reset registers 0 = PGOOD fault will reset registers	0
D3	reserved	do not write to this data bit	0
D2	reserved	do not write to this data bit	0
D1	General-Purpose Output (GPOP)	GPOP pin reflects the state of this bit	0
D0	General-Purpose Input (GPIP)	This bit reflects the state of the GPIP pin	0

Table 26 - Watchdog Timeout (R/W) - 07h

Bit	Function	Description	Reset State
D7	D7 of 8-bit watchdog timer	Watchdog timeout counter value (125ms increments), used in Software Mode only. FF = max value (32 sec) 01 = min value (125ms) 00 = reserved, do not use	1
D6	D6 of 8-bit watchdog timer		1
D5	D5 of 8-bit watchdog timer		1
D4	D4 of 8-bit watchdog timer		1
D3	D3 of 8-bit watchdog timer		1
D2	D2 of 8-bit watchdog timer		1
D1	D1 of 8-bit watchdog timer		1
D0	D0 of 8-bit watchdog timer		1

Table 27 - ADCIN Voltage (Read-Only) - 08h

Bit	Function	Description	Reset State
D7	D7 of 8-bit voltage measure	8-bit measurement of voltage at ADCIN pin (primary side). The A/D runs continuously with a 100Hz sampling rate (minimum), and can be read at full I^2C speed. FF (hex) = 2.5 V 00 (hex) = 0 V step size = 9.80 mV	0
D6	D6 of 8-bit voltage measure		0
D5	D5 of 8-bit voltage measure		0
D4	D4 of 8-bit voltage measure		0
D3	D3 of 8-bit voltage measure		0
D2	D2 of 8-bit voltage measure		0
D1	D1 of 8-bit voltage measure		0
D0	D0 of 8-bit voltage measure		0

Table 28 - ADCIN Alarm Threshold (R/W) - 09h

Bit	Function	Description	Reset State
D7	D7 of 8-bit A/D Interrupt Threshold	8 bit Threshold for A/D Alarm Interrupt (if enabled) from ADCIN input pin. FF (hex) = 2.5V 00 (hex) = 0 V step size = 9.80 mV	1
D6	D6 of 8-bit A/D Interrupt Threshold		1
D5	D5 of 8-bit A/D Interrupt Threshold		1
D4	D4 of 8-bit A/D Interrupt Threshold		1
D3	D3 of 8-bit A/D Interrupt Threshold		1
D2	D2 of 8-bit A/D Interrupt Threshold		1
D1	D1 of 8-bit A/D Interrupt Threshold		1
D0	D0 of 8-bit A/D Interrupt Threshold		1

Table 29 - System Clock Control (R/W) - 0Ah

Bit	Function	Description	Reset State
D7	reserved	do not write to this data bit	0
D6	reserved	do not write to this data bit	0
D5	reserved	do not write to this data bit	0
D4	reserved	do not write to this data bit	0
D3	PWM Clock Modulation Enable	1 = Clock modulation on 0 = off	1
D2	PWM Clock Modulation Type	1 = Fractional-n (see D1, D0 for modulation amount) 0 = Random (PRBS)	1
D1 D0	PWM Fractional-n Modulation Amount (not used for PRBS modulation)	D1, D0: 1,1 = reserved (do not use) 1,0 = 10% 0,1 = 5% 0,0 = 2%	1, 0 (10%)

Table 30 - Outputs 1, 2 Disable & Margin Control (R/W) - 0Eh

Bit	Function	Description	Reset State
D7	Output #2: Disable Control	0 = Normal output operation, with bits D6, D5, D4 defining margining operation. 1 = Output #2 is disabled.	0
D6 D5 D4	Voltage Margin for Output #2	D6, D5, D4 (with D7=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0
D3	reserved	do not write to this bit	0
D2 D1 D0	Voltage Margin for Output #1	D2, D1, D0: 1,1,1 = reserved, do not use 1,1,0 = reserved, do not use 1,0,1 = reserved, do not use 1,0,0 = +5% 0,1,1 = +2.5% 0,1,0 = -2.5% 0,0,1 = -5% 0,0,0 = no margining	0,0,0

Table 31 - Outputs 3, 4 Disable & Margin Control (R/W) - 0Fh

Bit	Function	Description	Reset State
D7	Output #4: Disable Control	0 = Normal output operation, with bits D6, D5, D4 defining margining operation. 1 = Output #4 is disabled.	0
D6 D5 D4	Voltage Margin for Output #4	D6, D5, D4 (with D7=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0
D3	Output #3: Disable Control	0 = Normal output operation, with bits D2, D1, D0 defining margining operation. 1 = Output #3 is disabled.	0
D2 D1 D0	Voltage Margin for Output #3	D2, D1, D0 (with D3=0): 1,1,1 = -2% 1,1,0 = -4% 1,0,1 = -6% 1,0,0 = -8% 0,1,1 = +6% 0,1,0 = +4% 0,0,1 = +2% 0,0,0 = no margining	0,0,0

Figure 24 - Typical Four Output Isolated Synchronous Flyback Application, VIN (max) ≤ 57V

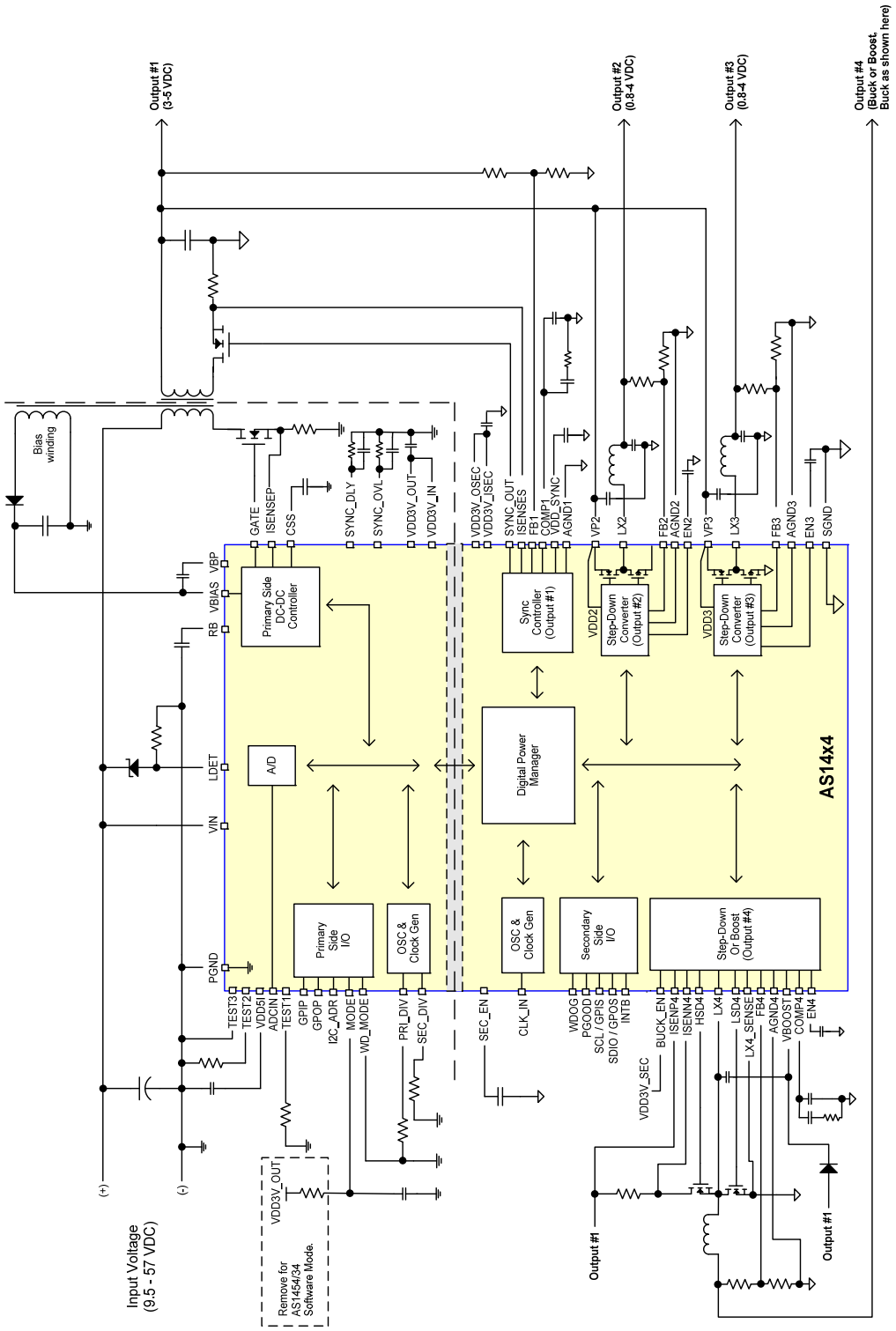
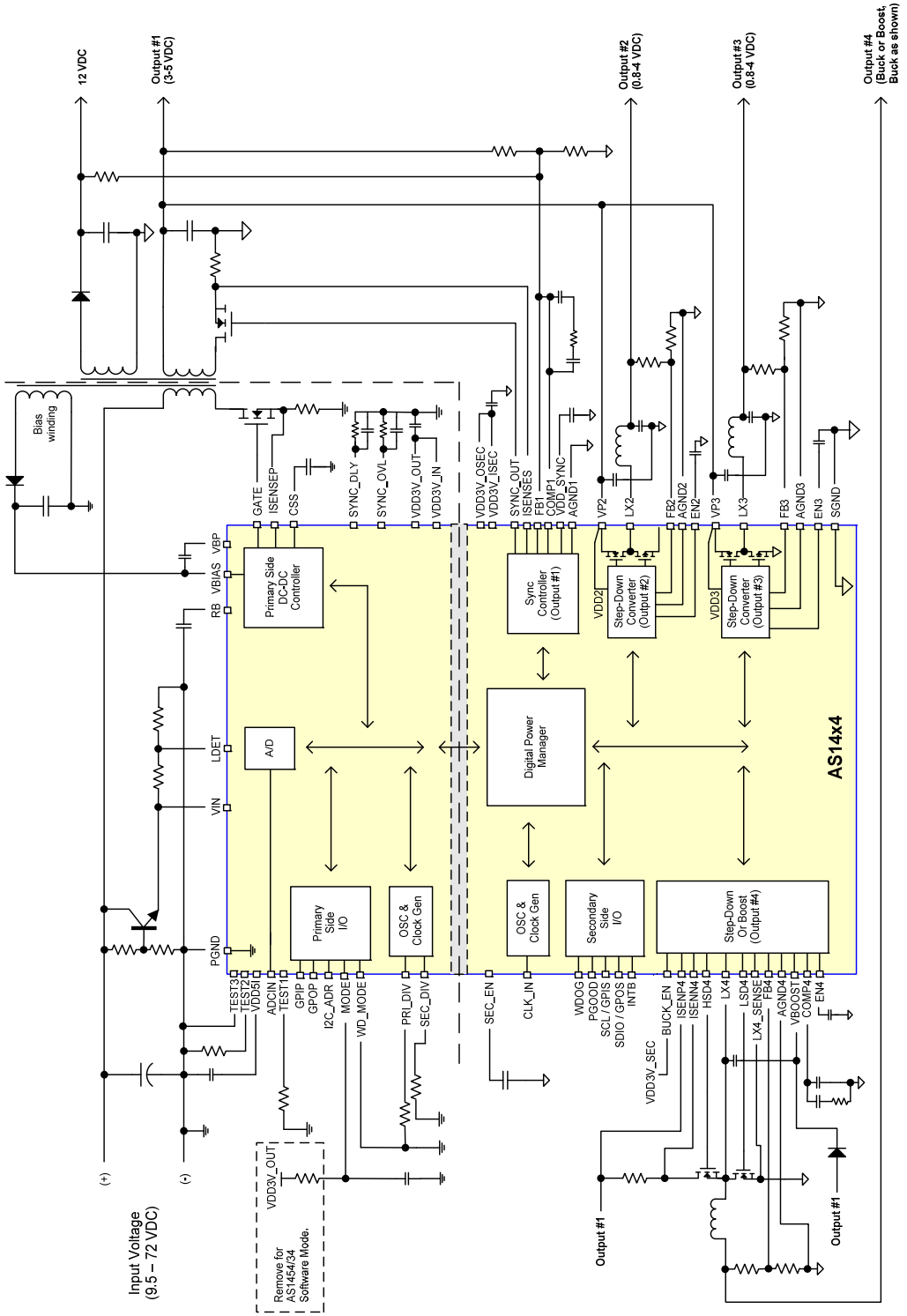
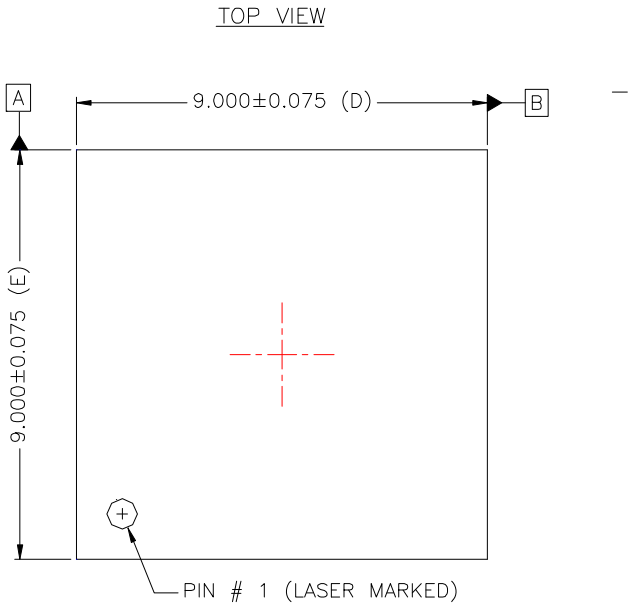


Figure 25 - Typical Five Output Isolated Synchronous Flyback Application, VIN (max) > 57V

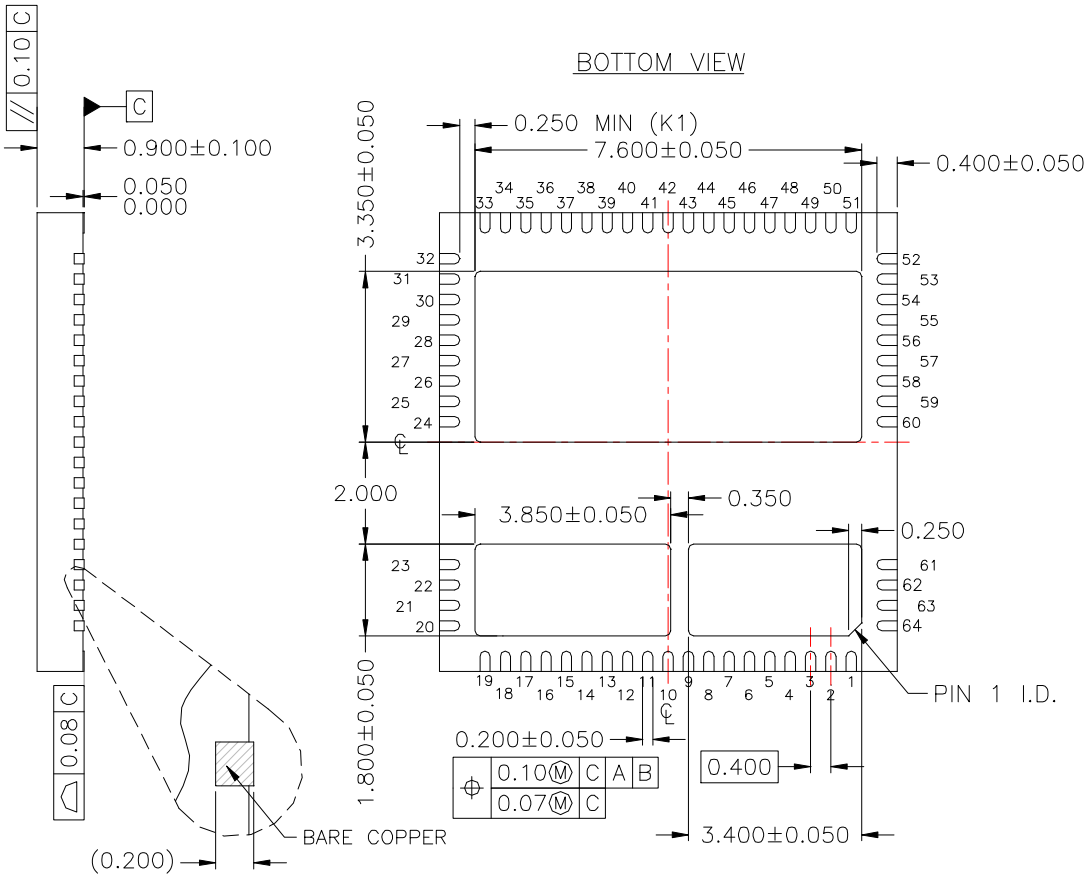


PACKAGE SPECIFICATIONS

Figure 26 - 64-Pin QFN Dimensions



NOTE :
1. Controlling Dimensions in mm.
2. REFER TO JEDEC MO-220 FOR DIMENSION NOT SHOWN HERE.
3. AVAILABLE LEADFRAME PART NUMBER : 16-064-374.


BOTTOM VIEW
0.10 C
C
0.900±0.100
0.050
0.000
0.08 C
(0.200)
BARE COPPER
3.350±0.050
1.800±0.050
2.000
0.250 MIN (K1)
7.600±0.050
0.400±0.050
3.850±0.050
0.350
0.250
0.200±0.050
0.10 M C A B
0.07 M C
0.400
3.400±0.050
PIN 1 I.D.

Contact Information

Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250
San Jose, CA. 95119
USA

Tel: (408) 746 9000
Fax: (408) 746-9391
Email inquiries: marcom@akrossilicon.com
Website: http://www.akrossilicon.com

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