AS1113 — 13W Powered Device with Integrated DC-DC Controller

GENERAL DESCRIPTION

The AS1113 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE). Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security and Web Cameras, Analog Telephone Adapters (ATA) and Point of Sales Terminals.

The AS1113 provides the functions required for power over Ethernet Powered Device (PD) applications.

The AS1113 integrates rectification and protection circuitry, a PD controller, and a DC-DC controller. This high level of integration provides significant reliability and protection advantages.

The AS1113 integrates rectification and protection circuitry, a PD controller, and a DC-DC converter. This high level of integration provides faster ressponse to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device. The device is designed to provide a safe low impedance discharge paths directly back to the earth ground, resulting in superior reliability and circuit protection.

AS1113 has been architected and designed to address both EMI emission concerns and surge/over-voltage protection in POE applications. The device implements many design features that minimizes transmission of system common-mode noise on to the UTP cable.

By using high-volume standard CMOS technology, Akros enables its customers to implement higher performance PoE devices with low cost and a small footprint.

FEATURES

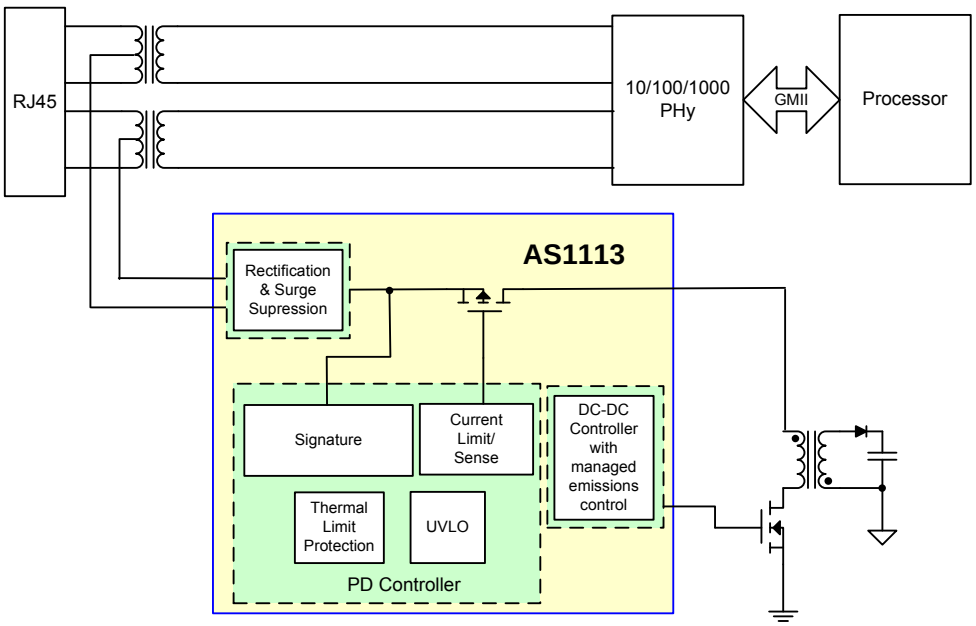
The AS1113 is fully integrated and architected at a system level to provide the following features:

- Fully supports *IEEE*® Std. 802.3af-2003
- Complies with IEC 61000-4-2/3/4/5/6 requirements
- Complies with IEC 60950 over-voltage protection requirements
- Integrated rectification for superior high voltage protection
- Integrated DC-DC controller provides superior EMI performance
- Provides seamless support for local power
- Over temperature protection
- Industrial temperature range, -40 ºC to +85ºC
- 5x5 mm, 20 pin QFN Package, RoHS compliant

TYPICAL APPLICATIONS

- Voice over IP (VoIP) phones
- Wireless LAN Access Points
- Pan, Tilt and Zoom (PTZ), security and Web Cameras
- Analog Telephone Adapters (ATA)
- Point of Sale (PoS) Terminals

SIMPLIFIED APPLICATION DIAGRAM



Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250, San Jose, CA 95119 USA
408.746.9000 ▪ www.AkrosSilicon.com

TABLE OF CONTENTS

GENERAL DESCRIPTION 1
TYPICAL APPLICATIONS 1
SIMPLIFIED APPLICATION DIAGRAM 1
FEATURES 1
TABLE OF CONTENTS 2
FIGURES 3
TABLES 3
PIN ASSIGNMENTS AND DESCRIPTIONS 4
TYPICAL PERFORMANCE CHARACTERISTICS 8
FUNCTIONAL DESCRIPTION 11
OVERVIEW OF POE 11
THE AS1113 POE DESIGN 11
POWER FEED ALTERNATIVES FOR 10/100 SYSTEMS 12
AS1113 OVERVIEW 13
RECTIFICATION & PROTECTION 14
PD CONTROLLER 14
MODES OF OPERATION 14
RESET 14
SIGNATURE DETECTION MODE 14
CLASSIFICATION MODE 14
IDLE MODE 15
ON STATE 15
LOCAL POWER MODE 15
PD CONTROL POWER AND THERMAL PROTECTIONS 15
UNDER VOLTAGE LOCKOUT (UVLO) 15
INRUSH CURRENT OPERATION 15
CURRENT LIMIT/CURRENT SENSE 15
THERMAL LIMIT PROTECTION 15
POE POWER-ON STARTUP WAVEFORM 16
DC-DC CONTROLLER 17
OVERVIEW 17
CURRENT-LIMIT/CURRENT SENSE 17
LOW LOAD CURRENT OPERATION 17
COMPENSATION AND FEEDBACK 17
SOFT-START INRUSH CURRENT LIMIT 17
AUXILIARY POWER OPTION 17
DC-DC CONVERTER TOPOLOGIES 17
FLYBACK VS. FORWARD OPERATION 17
BUCK OPERATION 17
PRIMARY SWITCHING TOPOLOGY 17
BOARD LAYOUT CONSIDERATIONS 18
APPLICATION CIRCUITS 19
PHYSICAL DIMENSIONS 21
CONTACT INFORMATION 22
IMPORTANT NOTICES 22
LEGAL NOTICE ..... 22#

FIGURES

Figure 1 - AS1113 Pin Diagram ..... 4#
Figure 2 - DC Current Limit vs. Junction Temperature ..... 8#
Figure 3 - Switch R_{ON} vs. Junction Temperature (Min/Max V_{IN}) ..... 8#
Figure 4 - Full Load Diode Bridge V_F vs. Junction Temperature ..... 8#
Figure 5 - Error Amplifier Ref. Voltage vs. Junction Temperature ..... 8#
Figure 6 - VDD5 vs. Junction Temperature ..... 9#
Figure 7 - VDD5 vs. Vin ..... 9#
Figure 8 - VBN & VBP (VBP wrt VDD480) vs Junction Temperature ..... 9#
Figure 9 - VBN & VBP (VBP wrt VDD48O) vs. Vin ..... 9#
Figure 10 - DCDC Load Regulation vs. I_{OUT} @V_{IN}=48V, V_O=12V ..... 10#
Figure 11 - DCDC Efficiency vs. I_{OUT} @V_{IN}=48V, V_O=12V ..... 10#
Figure 12 - DCDC Line Regulation @I_{OUT}=0.25A ..... 10#
Figure 13 - DCDC Efficiency vs. P_{OUT} @V_{IN}=48V, V_O=12V ..... 10#
Figure 14 - IEEE® Std. 802.3af-2003 Power Feeding Schemes for 10/100 Systems ..... 12#
Figure 15 – Top-Level Block Diagram of the AS1113 ..... 13#
Figure 16 – AS1113 LVMODE Connection ..... 15#
Figure 17 - *Representative Power-On waveform* ..... 16#
Figure 18 – AS1113 PCB Footprint ..... 18#
Figure 19 – 10/100M with Flyback DC-DC converter ..... 19#
Figure 20 – 10/100M with Forward DC-DC converter ..... 20#
Figure 21 – 10/100M with Buck DC-DC converter ..... 20#

TABLES

Table 1 – Pin Assignments ..... 4#
Table 2 – Absolute Maximum Ratings ..... 5#
Table 3 - Normal Operating Conditions ..... 5#
Table 4 - Electrical Characteristics ..... 6#
Table 5 - Package Thermal Characteristic ..... 7#
Table 6 - PoE Requirements ..... 11#
Table 7 - Classification Map ..... 14#

PIN ASSIGNMENTS AND DESCRIPTIONS

Figure 1 - AS1113 Pin Diagram

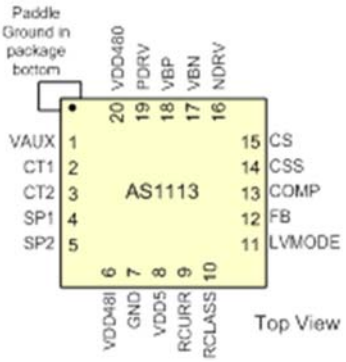


Table 1 – Pin Assignments

Pin	I/O	Name	Description
1	P	VAUX	Auxiliary supply input
2	P	CT1	High voltage supply transformer center tap input. Polarity insensitive.
3	P	CT2	High voltage supply transformer center tap input. Polarity insensitive.
4	P	SP1	High voltage supply from spare pair. Polarity insensitive.
5	P	SP2	High voltage supply from spare pair. Polarity insensitive.
6	O	VDD48I	Internal 48V bus pin. This pin is the positive bus after the input diode bridge. The bus is brought out to a pin for the connection of an external ESD capacitor (100nF) and signature resistor (26.7k Ω).
7	I	GND	Must be connected to paddle ground (not connected internally to the paddle).
8	O	VDD5	Internal 5 volts decoupling point
9	I	RCURR	Current limit resistor connection. Connect to paddle ground.
10	A	RCLASS	Classification resistor connection
11	A	LVMODE	Low Voltage Mode. When pulled high, LVMODE opens the internal FET switch and activates the DC-DC controller. Voltage threshold = 2.3V
12	A	FB	DC-DC Controller feedback point
13	A	COMP	DC-DC Controller error amplifier compensation network connection
14	A	CSS	DC-DC Controller soft-start capacitor
15	A	CS	DC-DC Controller peak current sense input (low side)
16	O	NDRV	DC-DC Controller N-MOSFET gate drive
17	O	VBN	DC-DC Controller low side supply decoupling
18	O	VBP	DC-DC Controller high side supply decoupling
19	O	PDRV	DC-DC Controller P-MOSFET gate drive
20	P	VDD48O	Switched 48V supply output
Paddle	P	GND	Local ground. This is the negative output from the diode bridge, and is not isolated from the line input

Key:

I = Input	PD = Internal pull-down
O = Output	A = Analog signal
I/O = Bidirectional	P = Power

Table 2 – Absolute Maximum Ratings

Description	Max Value	Units
High voltage pins (1—VAUX; 2 & 3—CT1 and 2; 4 & 5—SP1 and 2; 6—VDD48I; 18—VBP; 19—PDRV; 20—VDD48O)	60	Volts
Low voltage pins (8—VDD5; 10—RCLASS; 12—FB; 13—COMP; 14—CSS; 15—CS; 16—NDRV; 17—VBN, 11-LVMODE)	6	Volts
ESD Rating:		
Human body model[2]	2	kV
ESD charged device model	500	V
System level (contact/air) at RJ-45	8/15	kV
Temperature		
Storage Temperature	165	°C
Junction Temperature	150	°C

Unless otherwise noted, specifications are for the range of Ta = -40°C to +85°C and VIN = 48V.

[1] Absolute maximum rating is limits beyond which damage to the device may occur.

[2] The human body model is as described in JESD22-A114.

Table 3 - Normal Operating Conditions

Description	Min	Typical[1]	Max
V_{in}	36V	48V	57V
Operating temperature range	-40°C		85°C

[1] Typical specification; not 100% tested. Performance guaranteed by design and/or other correlation methods.

Table 4 - Electrical Characteristics

Description	Min	Typical[1]	Max	Units	Comments
PD Section					
Inrush Current Limit		200		mA	Initial inrush current
Current limit	400			mA	
Max. operating current		350		mA	
Switch On Resistance, R_{DS-ON}		1.5	2.0	Ω	
Diode bridge V_f forward voltage		900		mV	Single diode drop. Total bridge voltage drop includes 2 diodes.
Reset voltage level	0		2.7	V	
Min Signature voltage			2.7	V	
Max Signature voltage	10.1		14.5	V	
Min Classification voltage			14.5	V	In classification, the AS1113 sinks current as defined in table 5
Max Classification voltage	20.5			V	
Full power activation threshold	42			V	
Full power de-activation threshold	30		36	V	
Auxiliary power input voltage range	42		57	V	Auxiliary power applied between VAUX and GND. Applying power at both auxiliary and line inputs is not recommended. If both sources are present, the larger voltage will be used.
Input current for enable	TBD				
Input Current for disable	TBD				
MPS magnitude	TBD				
DC-DC Controller Section					
F_{OSC} (SMPS) switching frequency	325	350	375	kHz	Controller operating frequency
F_{OSC} Temperature Coefficient		0.12		%/C	
PDRV R_{OUT}		1.5	4.5	Ω	High side output drive resistance
NDRV R_{OUT}		1.2	3	Ω	Low side output drive resistance
PDRV and NDRV Gate Drive V_{OH} - V_{OL}	4.5		6	V	
Gate Drive Dynamic Response PDRV T_R, T_F NDRV T_R, T_F		 2.2 2		 nS nS	10% - 90% with C_{Load} = 1 nF
V_{PK}, peak current sense threshold voltage at CS	500	600	700	mV	Ipeak=Vpk/Rsense
Max. duty cycle		80		%	Internally limited
Min. duty cycle		6		%	Internally limited
VBN		4.7		V	Low side internal supply voltage; sets V_{OH} of NDRV
VBP (relative to VDD48O)		-5		V	High side internal supply voltage; sets V_{OL} of PDRV.
Error amplifier reference voltage	1.45		1.55	v	Compared to input of the FB pin

Soft start ramp time		2		ms	Conditions: CSS=100nF
COMP source current		30		µA	FB = 0V, COMP=0V
COMP sink current		30		µA	FB = 5V, COMP=5V
Open loop voltage gain		80		dB	
Small signal unity gain bandwidth		5		MHz	COMP connected to FB.
FB leakage (source or sink)		1		µA	0V>FB>4.5V
Local Power Mode					
LVMODE Threshold	2.1		2.4	V	
LVMODE Hysteresis		100		mV	
LVMODE Operating Voltage	10		57	V	
Thermal Protection					
Thermal shutdown temperature		165		°C	Above this Temp., the AS1113 is disabled.
Max. on-die operating temperature		140		°C	
Current reduction temperature threshold		145		°C	Temperature at which thermal current reduction is applied
Thermal current reduction		50		%	
Thermal current reduction hysteresis		20		°C	Temperature change required to restore full operation after thermal current reduction
Thermal shutdown hysteresis		40		°C	Temperature change required to restore full operation after thermal shutdown

[1] Typical specification is not 100% tested. Performance guaranteed by design and/or other correlation methods

Table 5 - Package Thermal Characteristic

Description	Min	Typical[1]	Max	Units	Comments
Thermal Resistance, Junction to Ambient, θ_{JA},		31		ºC/W	20 lead QFN package
Power Dissipation, P_{DISS}		1.5		W	At 12 W power delivery (12V output at 1A)

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2 - DC Current Limit vs. Junction Temperature

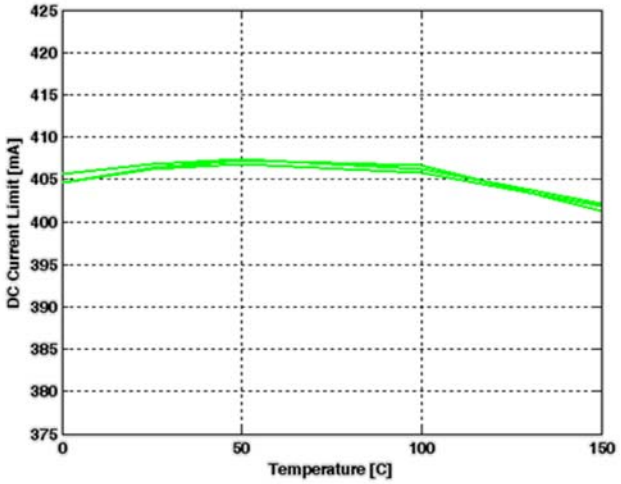


Figure 3 - Switch R_{ON} vs. Junction Temperature (Min/Max V_{IN})

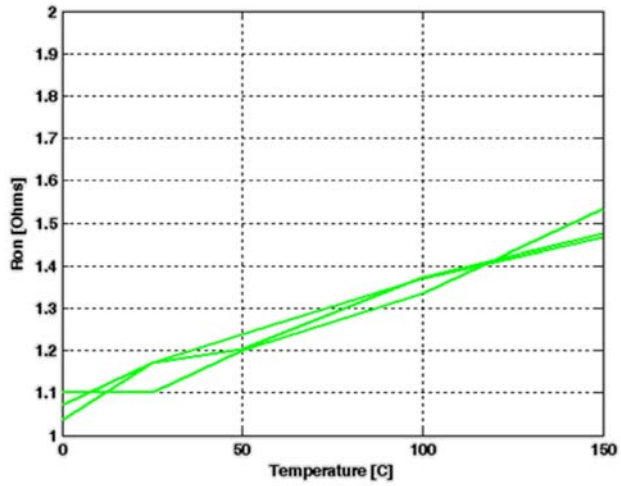


Figure 4 - Full Load Diode Bridge V_F vs. Junction Temperature

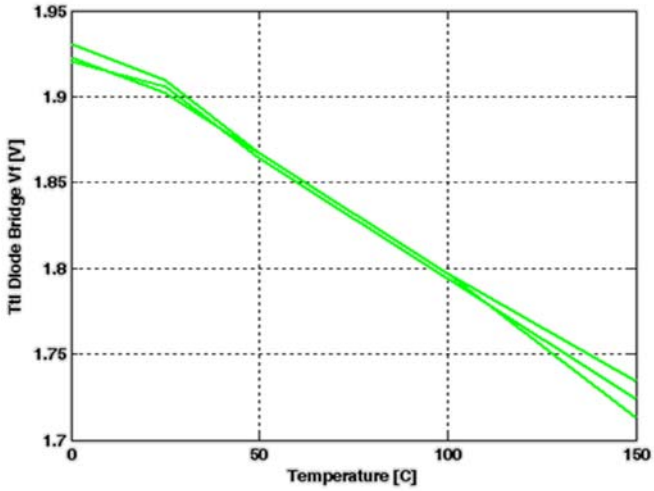


Figure 5 - Error Amplifier Ref. Voltage vs. Junction Temperature

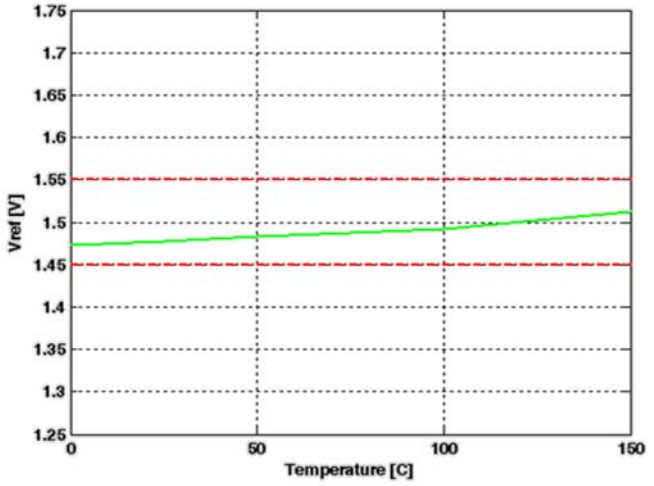


Figure 6 - VDD5 vs. Junction Temperature

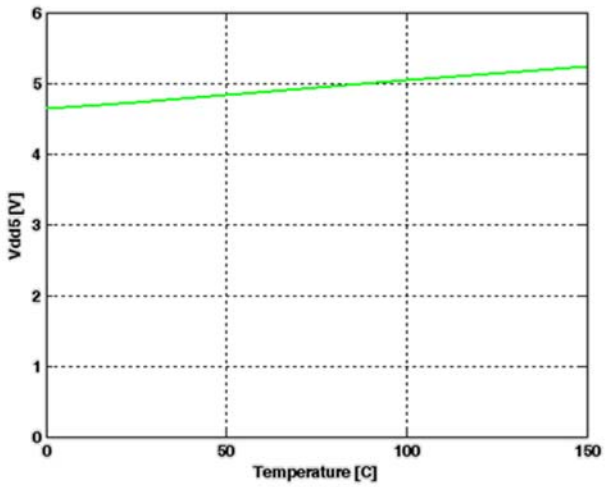


Figure 7 - VDD5 vs. Vin

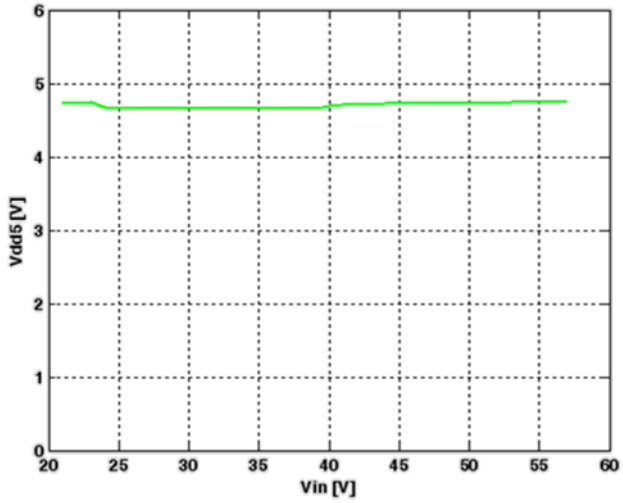


Figure 8 - VBN & VBP (VBP wrt VDD480) vs Junction Temperature

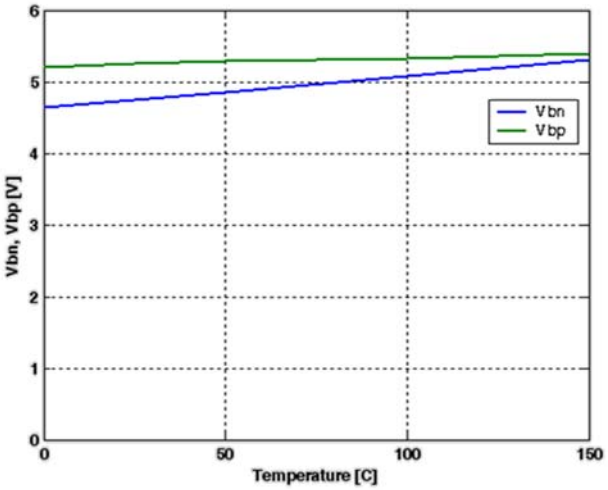


Figure 9 - VBN & VBP (VBP wrt VDD48O) vs. Vin

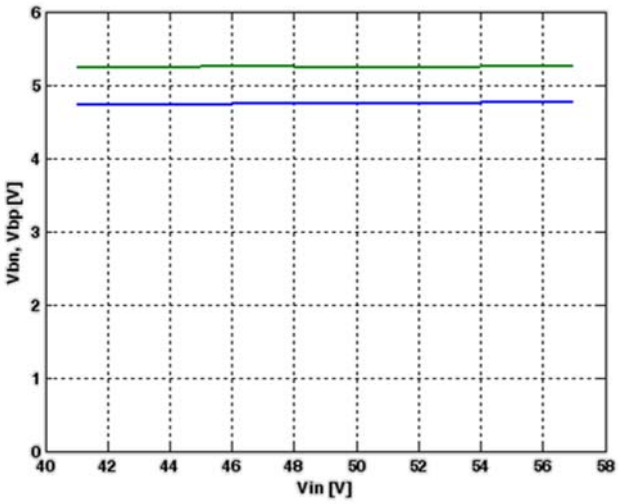


Figure 10 - DCDC Load Regulation vs. I_{OUT} @V_{IN}=48V, V_O=12V

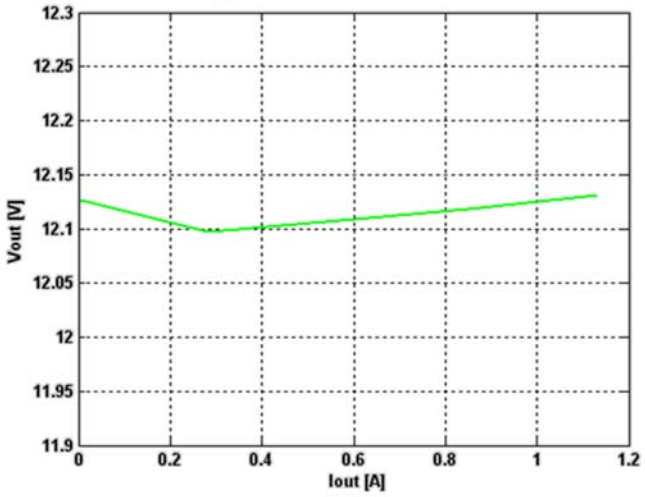


Figure 11 - DCDC Efficiency vs. I_{OUT} @V_{IN}=48V, V_O=12V

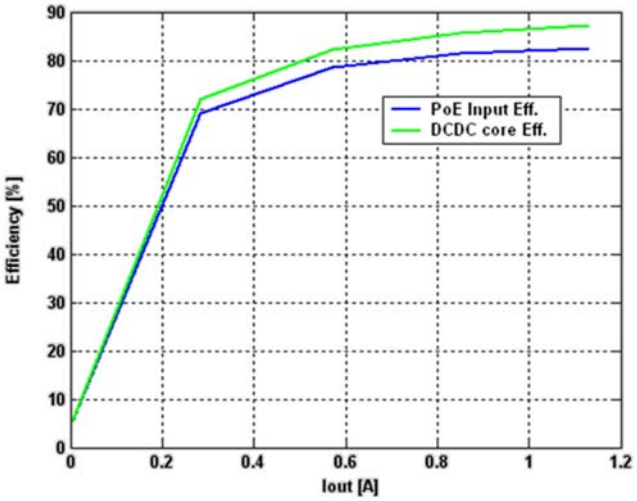


Figure 12 - DCDC Line Regulation @I_{OUT}=0.25A

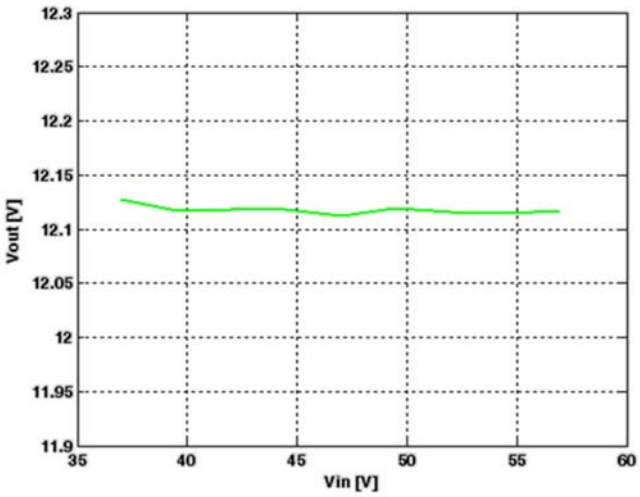
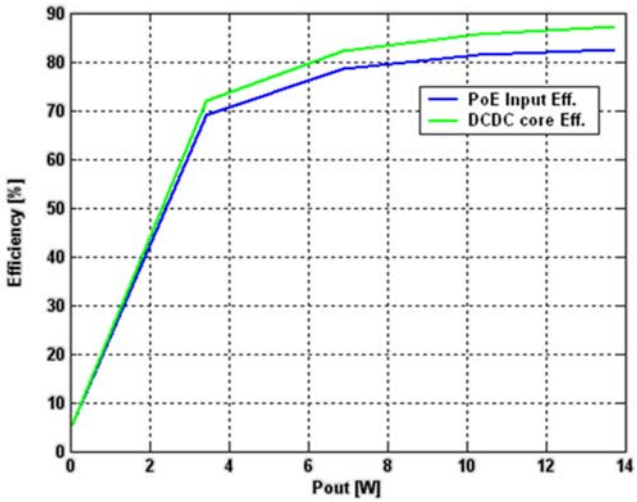


Figure 13 - DCDC Efficiency vs. P_{OUT} @V_{IN}=48V, V_O=12V



FUNCTIONAL DESCRIPTION

Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). The PoE standard *IEEE*® Std. 802.3af-2003 is intended to standardize the delivery of power over the Ethernet cables in order to accommodate remotely powered client devices. *IEEE*® Std. 802.3af-2003 defines a method for recognizing PDs on the network and supplying different power levels according to power level *classes* with which each PD is identified. By employing this method, designers can create systems that minimize power usage, allowing more devices to be supported on an Ethernet network.

The end of the link that provides power through the Ethernet cables is referred to as the power sourcing equipment (PSE). The powered device (PD) is the end of the link that receives the power. The PoE method for recognizing a PD and determining the correct power level to allocate uses the following sequence:

- *Reset*, wherein power is withdrawn from the PD if the applied voltage falls below a specified level.
- *Signature Detection*, during which the PD is recognized by the PSE.
- *Classification*, during which the PSE reads the power requirement of the PD. The Classification level of a PD identifies how much power the PD requires from the Ethernet line. This permits optimum use of the total power available from the PSE. (Classification is considered optional by *IEEE*® standard 802.3af-2003.)
- *ON* operation, during which the allocated level of power is provided to the PD.

This sequence occurs as progressively rising voltage levels from the PSE are detected.

To design PoE systems according to the PoE standard, designers have the following constraints:

Table 6 - PoE Requirements

Requirement	Value
Maximum power to the PD interface	13W
Voltage from PSE	44-57V
Maximum operating current	350mA
Line resistance	20Ω
Voltage drop due to series line resistance	7V
Min voltage at PD interface	36V

The AS1113 POE Design

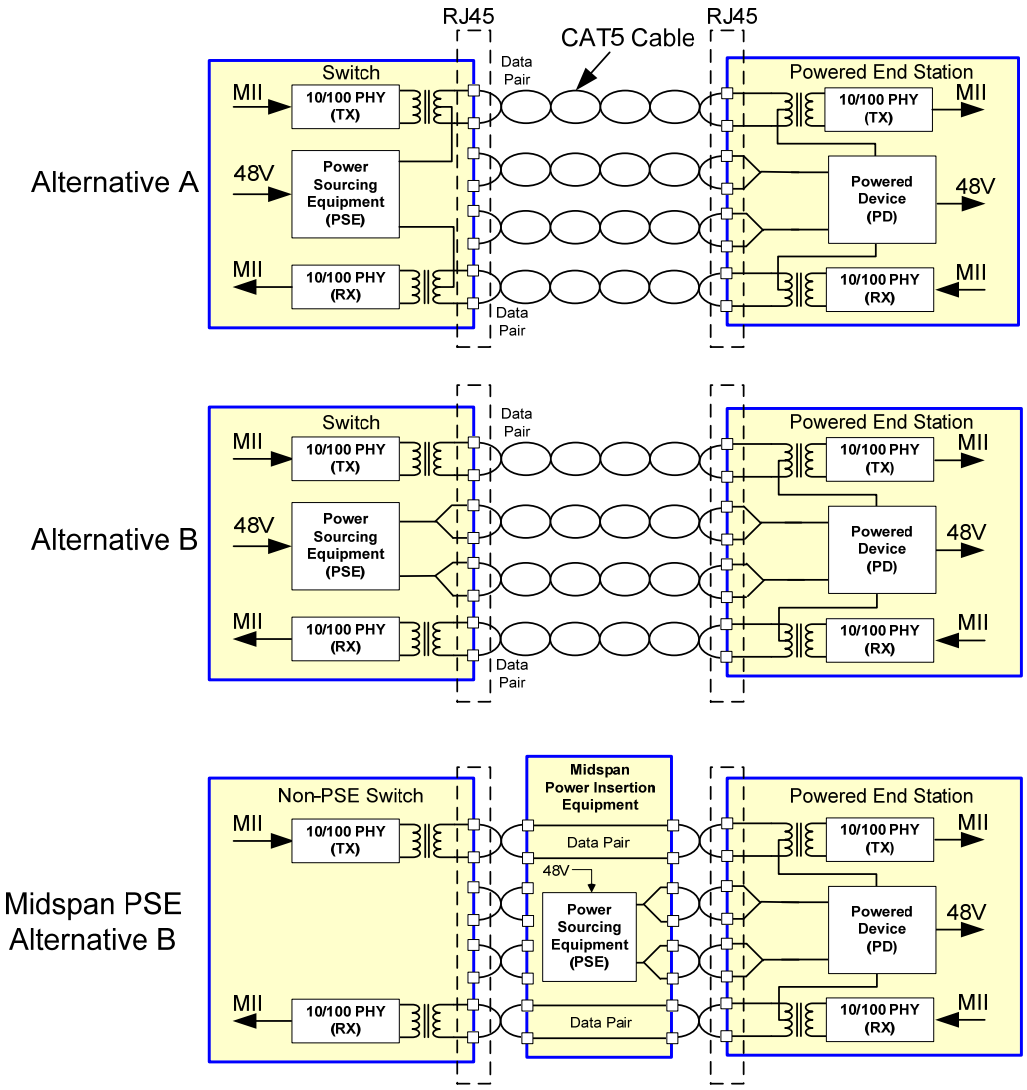
To help designers meet these requirements, the AS1113 is a fully integrated PoE PD controller. The AS1113 meets all system requirements for the *IEEE*® 802.3 standard for Ethernet and all power management requirements for *IEEE*® standard 802.3af-2003. The device have been designed and tested for compliance to international EMI standard (CISPR22, FCC Class B radiated emissions and EN55022 conducted emissions).

The AS1113 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. An integrated diode bridge is implemented to protect against polarity reversal, to provide alternative A and B detection and to provide improved protection to high voltage discharge. The AS1113 passes 2kV ESD tests, as well as 8kv Contact Discharge and 16.5 kV air Discharge tested per IEC61000-4.2, 4.4, 4.5

POWER FEED ALTERNATIVES FOR 10/100 SYSTEMS

Figure 13 illustrates the two power feed options allowed in the 802.3af standard for 10/100 systems. In Alternative A, a PSE powers the end station by feeding power along the twisted pair cable used for the 10/100 Ethernet signal via the center taps of Ethernet Transformers, on the line side of the transformers for the PD, power is delivered through pins1 and 2 and returned through pins3 and 6. In Alternative B, a PSE powers the end station by feeding power through the cable pairs not used for 10/100 data transmission. Power is delivered through pins 4, 5, 7 and 8 without transformers.

Figure 14 - IEEE® Std. 802.3af-2003 Power Feeding Schemes for 10/100 Systems

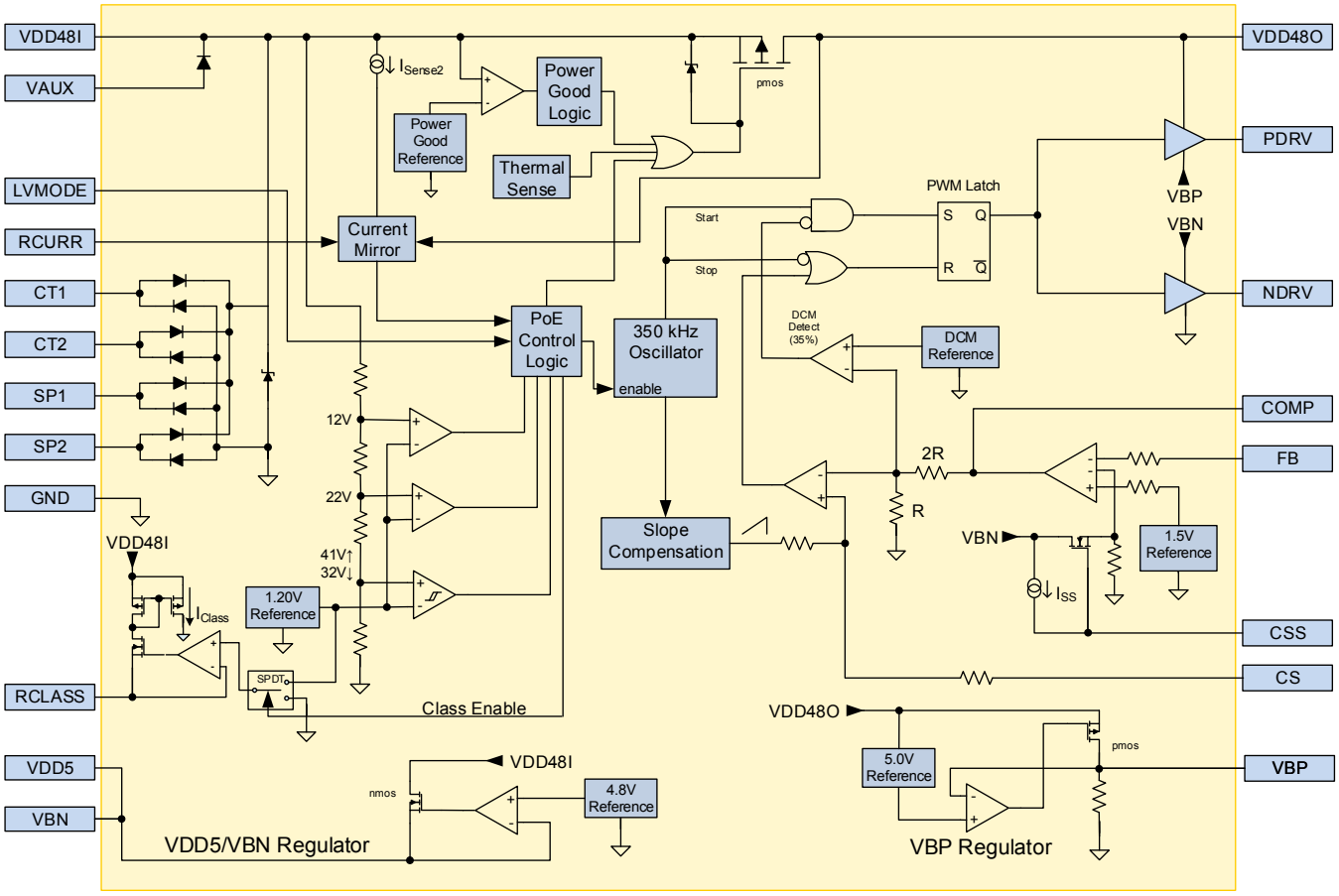


The *IEEE*® Std. 802.3af-2003 is intended to be fully compliant with all existing non- powered Ethernet systems. As a result, the PSE is required to detect via a well-defined procedure whether or not the connected device is PD compliant and classifies the needed power prior to applying power to the system. Maximum allowed voltage is 57V to stay within SELV (Safety Extra Low Voltage) limits.

AS1113 OVERVIEW

The AS1113 is a fully integrated PD that provides the functions required for power over Ethernet (PoE) applications. The optimized architecture of the AS1113 reduces external component cost in a small footprint while delivering high performance.

Figure 15 – Top-Level Block Diagram of the AS1113



RECTIFICATION & PROTECTION

To protect against polarity reversal and provide automatic polarity correction, the AS1113 includes an integrated bridge for rectification, with over voltage and transient protection, before passing to the switch and DC-DC controller.

PD Controller

The AS1113 PD Control interface is designed to provide full PD functionality for IEEE 802.3af compliant systems, with programmable support for the standard PD control functions.

The PD Control provides the following major functions:

1. Provides a resistance for signature detection.
2. Provides classification currents for power classification.
3. Provides PD full power.
4. Manages power and thermal protection overrides, including UVLO (under voltage lockout).

Modes of Operation

The AS1113 has five operating modes:

1. **Reset**—The classification state machine is reset, and all blocks are disabled.
2. **Signature Detection** —The PD signature resistance is applied across the input.
3. **Classification**—PD indicates power requirements to the PSE.
4. **Idle**—This state is entered after classification, and remains here until full-power input voltage is applied.
5. **ON**—The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the AS1113 transitions through the modes of operation in this sequence:

If no PSE is present, line voltage will be zero, which will hold the AS1113 in the reset state, and the AS1113 does not affect the Ethernet link function.

Reset

When the voltage supplied to the AS1113 drops below the signature voltage range (i.e. <2.7V), the chip will enter the reset state. In the reset state, the AS1113 consumes very little power.

Signature Detection Mode

During signature detection, the PSE applies a voltage to the AS1113 PD to read its power signature. The reading of the signature determines whether or not a PD is present and, if so, allows the PSE to determine the power class the PD belongs to.

To detect a PD, the PSE applies two voltages in the signature voltage range, and extracts a signature resistance value from the I-V slope. Valid resistance (I-V slope) values are between 23.75kΩ and 26.25kΩ. For the AS1113, signature resistance is generated by an external resistor between VDD48I and GND. Typically this is a 26.7kΩ, 1% resistor.

Classification Mode

Each class represents a power allocation level for a PD, so that PSE can manage power between multiple PDs. *IEEE*® Std. 802.3af-2003 defines classes of power levels for PDs as shown in Table 7.

To classify the PD, the PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the load current the PD sinks.

The AS1113 allows the user to program the classification current via an external resistor in the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 7.

Use the following equation to determine typical classification current:

$$I_{CLASS}[mA] = 2.0 + \frac{2360}{R_{CLASS}[k\Omega]}$$

Tolerance = Maximum of ±1.8mA or ±9%

- R_{CLASS} > 63.4kΩ

Table 7 - Classification Map

Class	Power (Watts)	Iclass	Rclass
0	0.44-12.95	0-4 mA	Pull-up, 1%
1	0.44-3.84	9-12 mA	280kΩ, 1%
2	3.84-6.49	17-20 mA	143kΩ, 1%
3	6.49-12.95	26-30 mA	90.9kΩ, 1%
4	Reserved	36-44 mA	63.4kΩ, 1%

Idle Mode

In the Idle mode, between Classification and the ON state, PD Current is limited to monitoring circuitry to detect the on-state threshold.

ON State

In the ON state, the AS1113 is supplying power.
At a voltage at or above 42V, the PD turns on and full power is available via the AS1113 DC-DC Controller.

Local Power Mode

The LV Mode Pin can be used in applications where the PD appliance draws power from either the Ethernet cable or a local external DC power source.

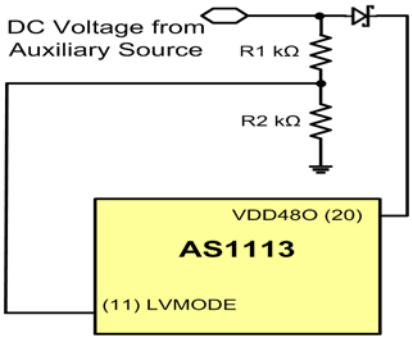
When pin11 is pulled high (> 2.3V), it will open the internal FET switch while the DC-DC converter remains operational. The local power should be injected at the VDD48O node, through an external Schottky diode. Refer to application circuits 8 & 9 for the connection details.

The maximum input voltage at the LVMODE pin should not exceed 6V. A resistive divider network should be used to divide down the LVMODE control voltage. Resistor values will depend on the voltage of the local power supply. The internal DC-DC converter will operate with input voltages ranging from 10V to 57V.

The LVMODE pin should only be used when the PD is configured for class 1-4. The LVMODE pin should not be used in class 0 applications.

If the LVMODE pin is pulled low, the PD will operate in a normal fashion, whereby the FET will open when the input voltage at VDD48I drops below the full power deactivation threshold.

Figure 16 – AS1113 LVMODE Connection



PD CONTROL POWER AND THERMAL PROTECTIONS

The AS1113 provides the following PD control power and thermal protections:

- Under Voltage Lockout (UVLO)
- Current Limit with integrated current sense
- Thermal Limit/Protection

Under Voltage Lockout (UVLO)

The AS1113 contains a line Under-Voltage Lockout (UVLO) circuit. The UVLO circuitry detects conditions when the supply voltage is too low (less than 36V), and disconnects the power to protect the PD.

Inrush Current Operation

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. Also, it helps prevent the PSE from going into a current limit mode.

Current Limit/Current Sense

The Current Limit/Current Sense circuitry minimizes on-chip temperature peaks by limiting inrush current and operating current. It monitors the current via an integrated sense circuit and regulates the gate voltage on an integrated low-leakage 80V power MOSFET. In addition, the power MOSFET can be shut down by the PD Controller subsection or the Thermal Limit Protection subsection.

Thermal Limit Protection

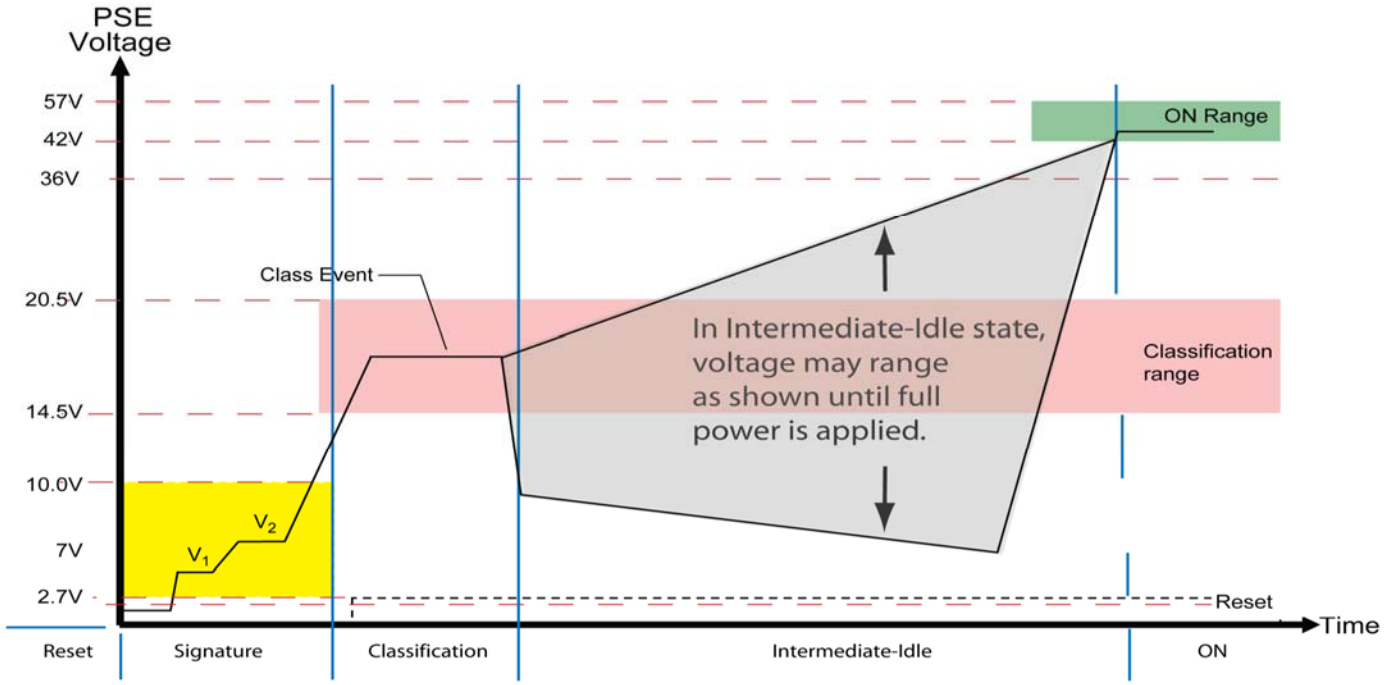
The AS1113 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent pre-set thermal limits from being exceeded.

Two-stage thermal current limiting is implemented, which reduces the operating current limit by 50% when the die temperature reaches 145˚C, and disables the power MOSFET switch above 165˚C. Normal current limits in both cases are reapplied when the die temperature returns to 125˚C.

POE POWER-ON STARTUP WAVEFORM

Figure 17 represents the power-on sequence for PoE operation. The waveform reflects typical voltages present at the PD-PI during signature, classification and power-on.

Figure 17 - *Representative Power-On waveform*



Notes

1. Items V1 and V2 on the drawing represent the points where most PSEs apply two voltages and extract a signature resistance value.
2. Class Event represents the point where the PSE takes a current reading to determine the class of the PD.

   During classification, the PSE presents a voltage between 14.5V and 20.5V. At this time, the PD presents a load current as determined by the resistance on the RCLASS pin.

   After the PSE measures the PD load current and determines that it can deliver the requested power, it moves into the ON state by raising the voltage above 42V.

DC-DC CONTROLLER

Overview

The DC-DC architecture is a current-mode controller which can be configured with external component changes to flyback, forward, or non-synchronous low-side switch buck topologies. Both non-isolated and isolated topologies are supported.

As part of full system level solution for EMI, Akros has focused significant effort in reducing switching noise in the integrated power converters through unique techniques of balancing the signaling of the FET drivers and reducing ground bounce by minimizing the dV/dt switching noise.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes soft-start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts up. The controller provides gate control signals to external switching MOSFETs, and uses an external resistor to sense the transformer primary current.

The DC-DC controller includes programmable soft start, 80% maximum duty cycle, fixed switching frequency and a voltage output error amplifier.

Current-Limit/Current Sense

The DC/DC controller provides cycle-by-cycle current limiting to ensure that transformer primary current limits are not exceeded. In addition, the maximum average current in the transformer primary is set by internal duty cycle limits.

Low Load Current Operation

The internal circuitry detects a low output power condition and puts the DC-DC Controller into a discontinuous current operation (DCM) mode.

Compensation and Feedback

For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the FB pin is shorted to ground. In these applications, the COMP pin is pulled up to 4.8V (nominally) by an internal current source. This pull-up can be the termination for an opto-isolator, or an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network senses the output voltage and is applied directly to the FB pin. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start Inrush Current Limit

The internal circuitry automatically ramps up the inrush current by limiting the maximum current allowed in the transformer primary magnetizing inductance per clock cycle. The amount of time required to perform a soft start cycle is determined by the CSS capacitor. A CSS capacitor of 100 nF provides approximately 2ms of soft startup ramp time.

AUXILIARY POWER OPTION

The Auxiliary Power Option allows the AS1113 to be powered from a DC power source, other than the Ethernet line. Examples of DC sources are AC/DC wall adapters, batteries, or solar cells. This feature may also be used, to supply power that exceeds the load capacity of the PSE, or in non-PoE systems.

DC-DC CONVERTER TOPOLOGIES

Flyback vs. Forward Operation

The DC-DC controller can be configured in several different operational topologies and in either isolated or non-isolated configurations. The FLYBACK mode is chosen when a minimum number of external components is desired or there is a large step-down and the output voltage is < 7V. The FORWARD mode is chosen with lower output noise and higher efficiency is desired. The FLYBACK mode is shown in Figure 8 and the FORWARD mode in shown in Figure 9, both in isolated configurations.

Buck Operation

The BUCK mode is shown in Figure 10. The buck mode is used only in non-isolated applications. The BUCK mode uses an inductor instead of a transformer and therefore has the smallest overall footprint. Figure 10 shows the BUCK converter in a non-synchronous operation where the output voltage is referenced to VDD48O. Since the FB voltage is ground referenced, the feedback signal must be level shifted back down to ground. This is accomplished by the two PNP transistors and the associated resistors.

Primary Switching Topology

The DC-DC controller uses a two-switch topology to minimize noise, maximize efficiency and reduce the breakdown requirements for the switching transistors. During OFF time and when the core is being reset, a snubbing circuit, consisting of parallel Schottky diodes, directs the transformer magnetizing current into the bulk storage capacitors connected to VDD48O. This additional snubbing circuitry minimizes the ringing that can occur on the primary winding of the power transformer. In single switch topologies, the maximum V_{DS} are approximately 2.5X VDD48O and there can be significant ringing during OFF time, when the transformer core is being reset. Again, snubbing circuitry is used to dissipate the ringing noise that occurs during the switching transitions.

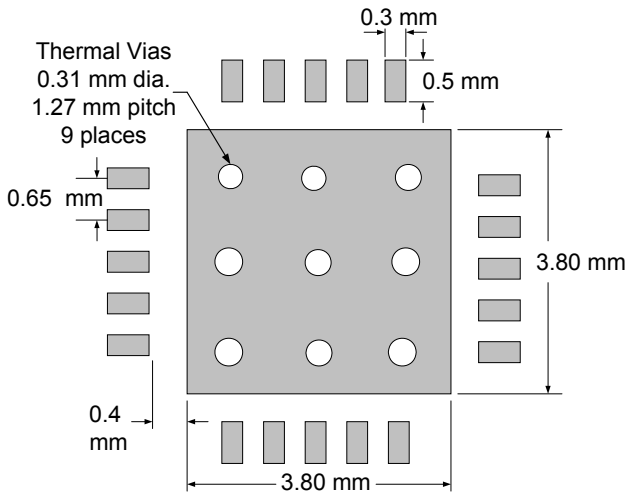
Board Layout Considerations

The AS1113 package uses an integral thermal pad to help dissipate heat from the switch and diode bridge. Designers must consider thermal design as an integral part of their systems design and remove heat via this pad.

For adequate heat dissipation, the board layout must include a ground pad which accomplishes both the ground connection and dissipates the heat energy generated by the PD. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB

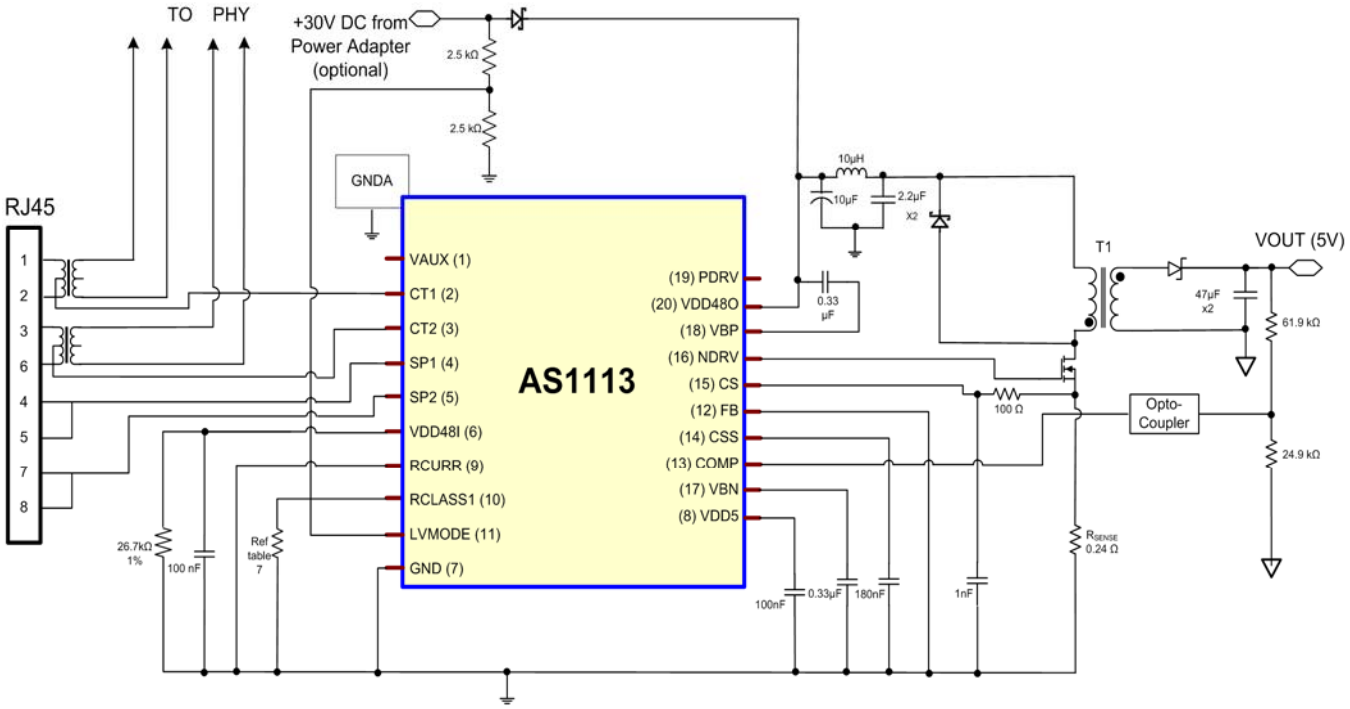
A typical PCB layout for the AS1113 is shown in Figure 17.

Figure 18 – AS1113 PCB Footprint



APPLICATION CIRCUITS

Figure 19 – 10/100M with Flyback DC-DC converter

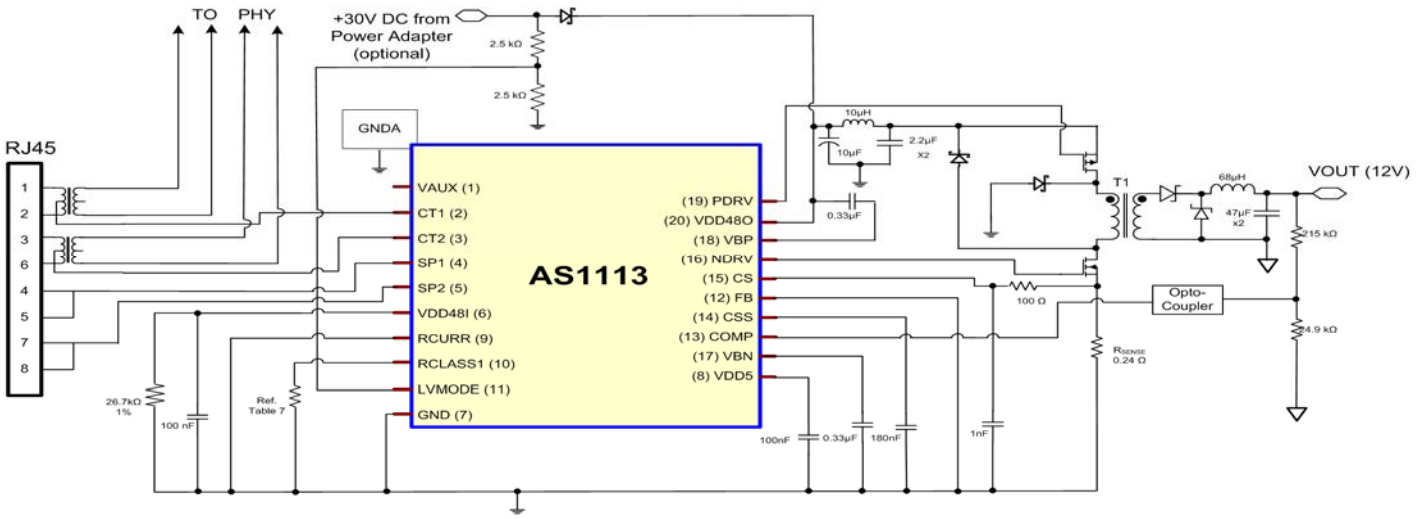


NOTES:

All resistors 1% except as otherwise noted

1. FET: Vishay Si7812
2. T1: Transtek POET0078. For applications that use local power < 30 V DC, work with the transformer manufactures to optimize the windings for low voltage operation
3. Primary side Schottky diodes: B1100-13
4. Secondary Side Schottky diodes: SS36
5. Opto-Coupler FOD2712

Figure 20 – 10/100M with Forward DC-DC converter

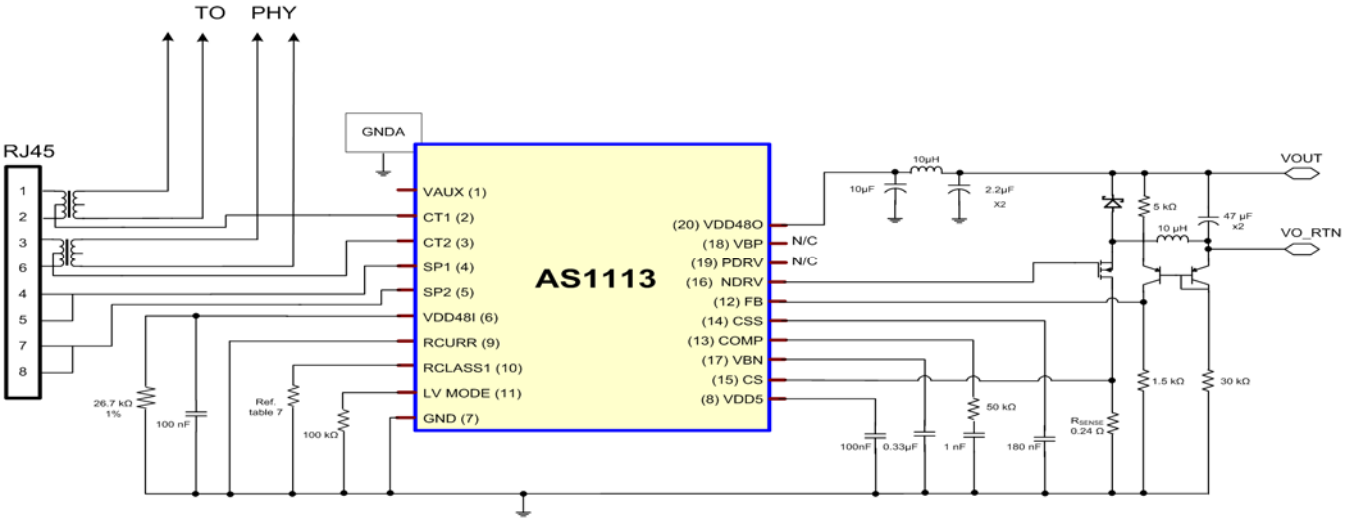


NOTES:

All resistors 1% except as otherwise noted

1. Dual FET: Vishay Si7530
2. T1: Transtek POET0072. For applications that use local power < 30 V DC, work with the transformer manufactures to optimize the windings for low voltage operation
3. Primary side Schottky diodes: B1100-13
4. Secondary Side Schottky diodes: SS36
5. Opto-Coupler FOD2712

Figure 21 – 10/100M with Buck DC-DC converter

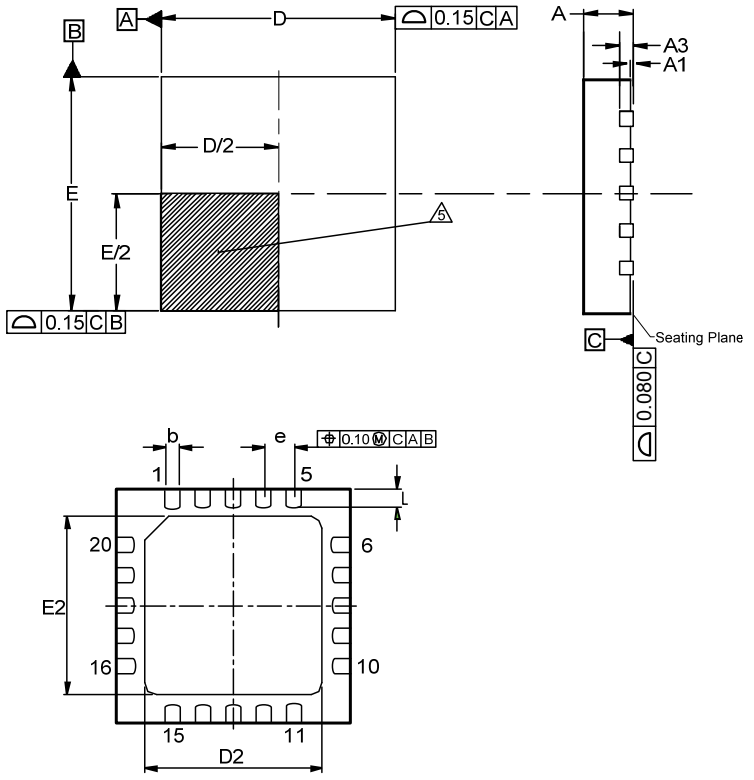


NOTES

1. All resistors 1% except as otherwise noted.
2. FET: Vishay Si7812
3. Schottky diode: MBRS320T3
4. PNP transistors: BC556
5. Remaining components are common resistors and capacitors.

PHYSICAL DIMENSIONS

Figure 21. 20 Pin QFN Package, 5mm X 5mm



Common Dimensions			
	MIN.	NOM.	MAX
A	0.80	0.85	0.95
A1	0.00	0.02	0.04
A3		0.20 REF.	
D	4.85	5.00	5.15
D2	3.70	3.80	3.90
E	4.85	5.00	5.15
E2	3.70	3.80	3.90
L	0.35	0.40	0.45
N		20L	
b	0.25	0.30	0.35
e		0.650 BSC	
JEDEC		MO-220-VHHC-2	

NOTES
1. Controlling dimensions in mm.
2. Dimension tolerances are ±0.1 (angular tolerance ±3°) unless otherwise specified.
3. All dimensions and tolerances conform to ANSI Y14.5M-1994.
4. Coplanarity applies to exposed pad as well as the terminals.
5. Pin 1 location may be identified by either a mold or marked feature.
6. JEDEC reference MO-220.

Contact Information

Akros Silicon, Inc.
6399 San Ignacio Avenue, Suite 250
San Jose, CA 95119
USA

Tel: (408) 746 9000
Fax: (408) 746-9391
Email inquiries: marcom@akrossilicon.com
Website: http://www.akrossilicon.com

Important Notices

Legal notice

Other names, brands and trademarks are the property of others.

Akros Silicon™ assumes no responsibility or liability for information contained in this document. Akros reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or services without notice. The information contained herein is believed to be accurate and reliable at the time of printing.

Reference design policy

This document is provided as a design reference and Akros Silicon assumes no responsibility or liability for the information contained in this document. Akros reserves the right to make corrections, modifications, enhancements, improvements and other changes to this reference design documentation without notice.

Reference designs are created using Akros Silicon's published specifications as well as the published specifications of other device manufacturers. This information may not be current at the time the reference design is built. Akros Silicon and/or its licensors do not warrant the accuracy or completeness of the specifications or any information contained therein.

Akros does not warrant that the designs are production worthy. Customer should completely validate and test the design implementation to confirm the system functionality for the end use application.

Akros Silicon provides its customers with limited product warranties, according to the standard Akros Silicon terms and conditions.

For the most current product information visit us at www.akrossilicon.com

Life support policy

LIFE SUPPORT: AKROS' PRODUCTS ARE NOT DESIGNED, INTENDED, OR AUTHORIZED FOR USE AS COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS. NO WARRANTY, EXPRESS OR IMPLIED, IS MADE FOR THIS USE. AUTHORIZATION FOR SUCH USE SHALL NOT BE GIVEN BY AKROS, AND THE PRODUCTS SHALL NOT BE USED IN SUCH DEVICES OR SYSTEMS, EXCEPT UPON THE WRITTEN APPROVAL OF THE PRESIDENT OF AKROS FOLLOWING A DETERMINATION BY AKROS THAT SUCH USE IS FEASIBLE. SUCH APPROVAL MAY BE WITHHELD FOR ANY OR NO REASON.

“Life support devices or systems” are devices or systems which (1) are intended for surgical implant into the human body, (2) support or sustain human life, or (3) monitor critical bodily functions including, but not limited to, cardiac, respirator, and neurological functions, and whose failure to perform can be reasonably expected to result in a significant bodily injury to the user. A “critical component” is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

SUBSTANCE COMPLIANCE

With respect to any representation by Akros Silicon that its products are compliant with RoHS, Akros Silicon complies with the Restriction of the use of Hazardous Substances Standard ("RoHS"), which is more formally known as Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. To the best of our knowledge the information is true and correct as of the date of the original publication of the information. Akros Silicon bears no responsibility to update such statement.

Revision:	Version 2.1
Release Date:	June 2, 2015